

Model Name: GA-X99-UD5 WIFI Rev 1.1

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04-06	CPU_LGA2011-DDR
07-08	CPU_LGA2011-CTRL_PCIE_DMI
09-10	CPU_LGA2011-PWR
11-12	DDR III CHANNEL A/B
13-14	DDR III CHANNEL C/D
15-16	PCH_SATA_GPIO_AUDIO
17	PCH_DMI_USB_PCIE_PCI
18	PCH_PWR_GND
20-21	PCI EXPRESS X16 SLOT_1/2
22	PCI EXPRESS X16 Switch
23-24	PCI EXPRESS X8 SLOT 1/2
25	PCI EXPRESS X1 SLOTS
26-27	CPU& PEG CLOCK BUFFER
28	ITE 8620 SIO
29	DUAL BIOS
30-31	VCORE IR3580
33-35	DDR A/B & VPP&DDRVTT IR3570*2
36	PCH CORE POWER RT8120
37-38	DISCRETE POWER
39	FP ,TPM ,THB
40	ATX , 80 PORT
41	I/O HWM ,FAN CTRL
42	ITE EC 8791
43	ITE EC 8951

SHEET TITLE

44	BUTTON & PROBE
45	EC HWM ,FAN CTRL
46	SOUND LEVEL SENSOR
47-48	M.2 WIFI & 10Gb SSD
49-52	USB3 HUB A/B
53-55	ALC1150+NE5532
56	USB3_LAN1/2 ,AUDIO JACK
57	PS2 , WIFI, HS BUTTON
58-59	LAN i210& i218
60	R_USB30
61	F_USB2 & F_USB3
62	PCH GPIO LIST
63	Parts Location

Model Name: GA-X99-UD5 WIFI

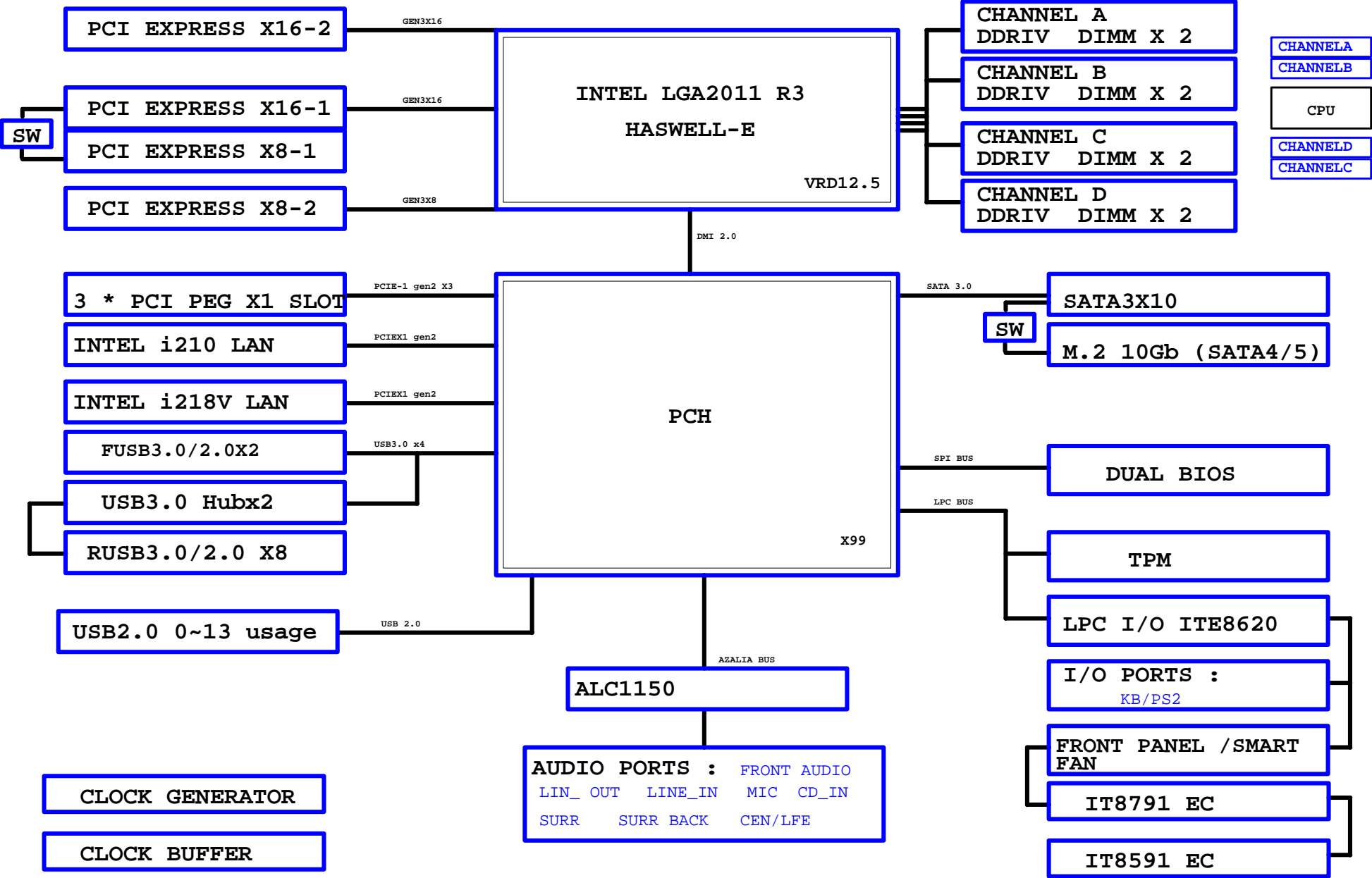
Component value change history

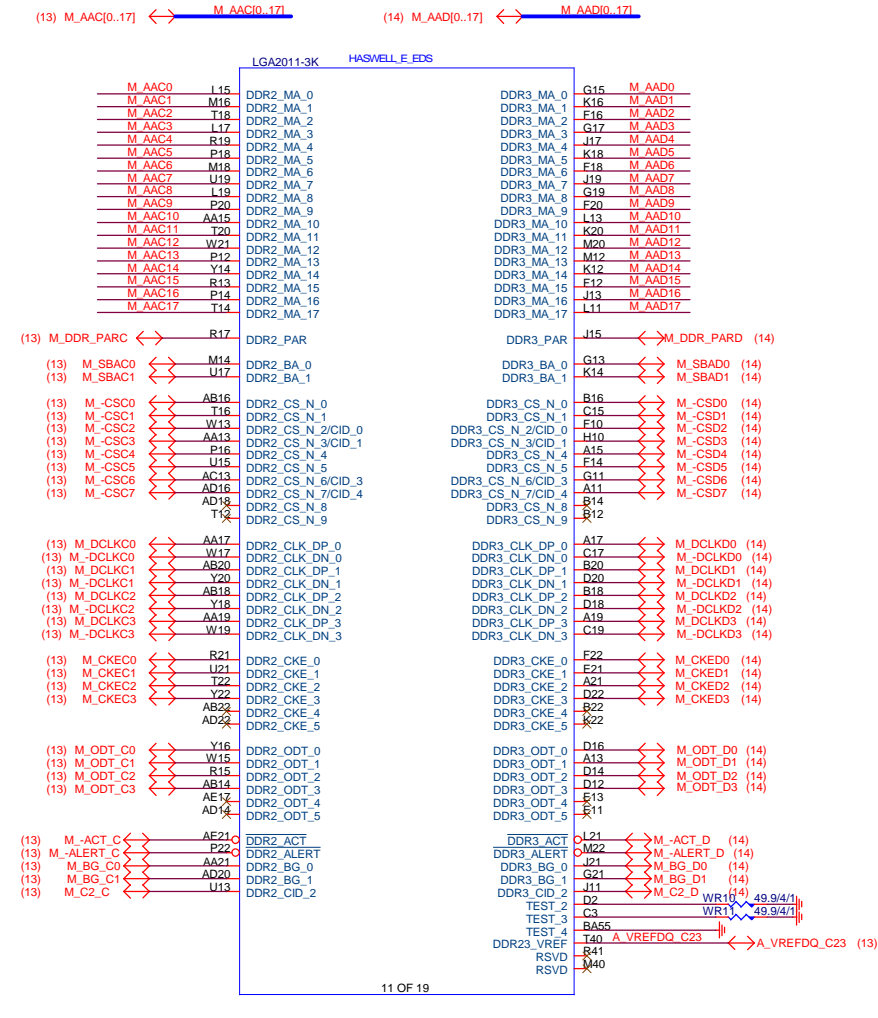
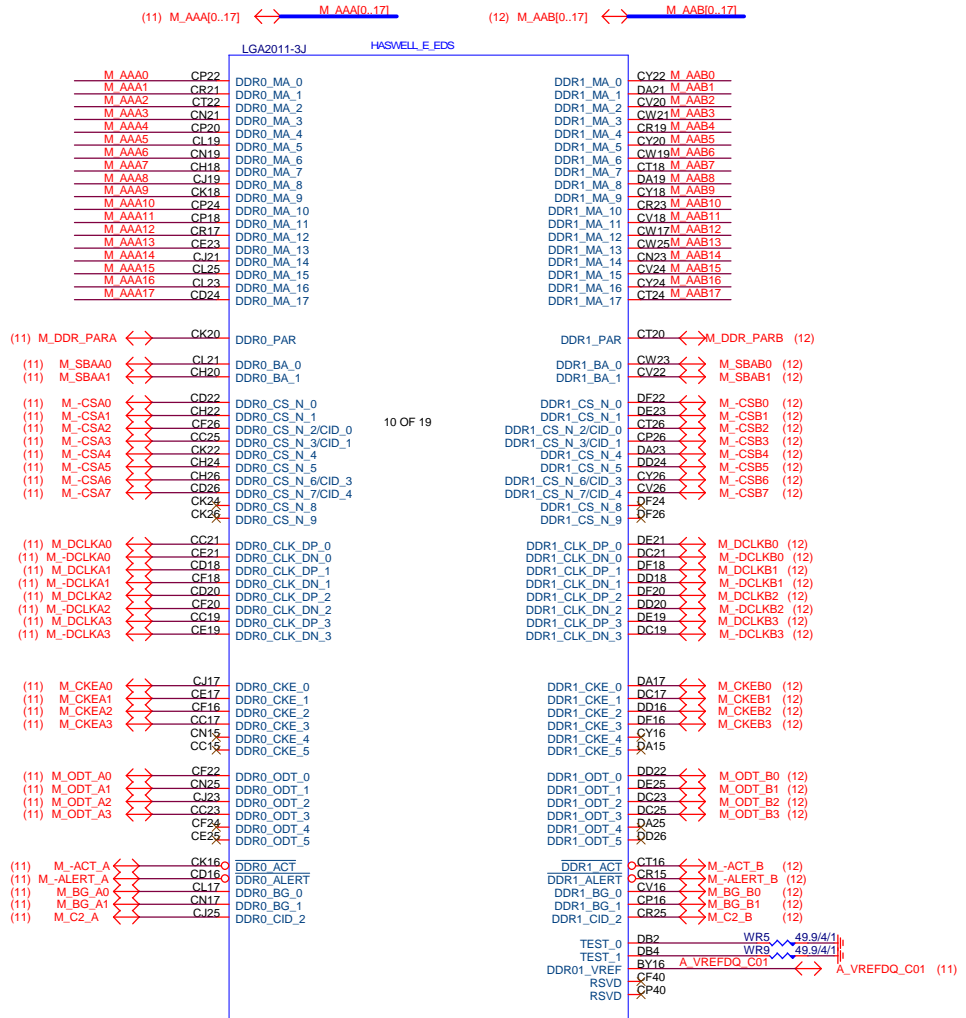
[illegible]

Circuit or PCB layout change

DATE	Change Item	Reason
2014/05/15 Rev 0.1	1. From GA-X99-Gaming G1 Rev 0.1 2. P53-P55 Creative change to ALC1150+NE5532 3. P58, E2201 change to i210 4. Remove P57 USB_DAC Power 5. VRM change to SMD Choke 0.15uH (In & Out) 6. SATA3_4_5 change to SATA Express 7. DDR12V Output choke change to SMD 0.3uH 8. SL_MIC1 & SL_MIC2改放背板 9. Audio use MW Cap 33uF+220uF(8*). 10. Add CQ33 & CQ34 for LED_CON1 & LED_CON2 11. N_ME_PWROK改成由RT9018 (U8)過來 12. UCF1 & UCF2至R_USB30的銅箔由2層增加為4層 13. MH1 change to GND. 14. ANTENNA_HOLD-3 change to -4 15. IC8-ATRC change to IC8-ATRC-1 16. M2_WIFI change to 2 parts, Footprint modify. 17. CEC11 change to 6x5 18. N_ME_PWROK circuit change	
2014/07/10	1. Modify from X99-UD7 WIFI Rev 0.2 2. 修改x99 note 152-179	Rev 0.1
2014/07/21	1.由X99-UD5 WIFI Rev 0.1來修改 2.PCIEX16_1 rename to PCIE_1 3.PCIEX16_2 rename to PCIE_2 4.PCIEX8_1 rename to PCIE_4 5.PCIEX8_2 rename to PCIE_3 6.PCIEX1_1 rename to PCIE_5 7.PCIEX1_2 rename to PCIE_6 8.PCIEX1_3 rename to PCIE_7 9.ECR142,ECR143 change to 0402 電阻 10.PE3_LED rename to PE2_LED 11.PE4_LED rename to PE3_LED 12.PE2_LED rename to PE4_LED 13.ITB_PH2 改回 pin header 14.DDR4_1_A1 rename to DDR4_1_1A 15.DDR4_2_A2 rename to DDR4_2_2A 16.DDR4_3_B1 rename to DDR4_3_1B 17.DDR4_4_B2 rename to DDR4_4_2B 18.DDR4_5_C1 rename to DDR4_5_1C 19.DDR4_6_C2 rename to DDR4_6_2C 20.DDR4_7_D1 rename to DDR4_7_1D 21.DDR4_8_D2 rename to DDR4_8_2D	Rev 1.0
2014/10/14	改x4顆粒 support	Rev 1.1

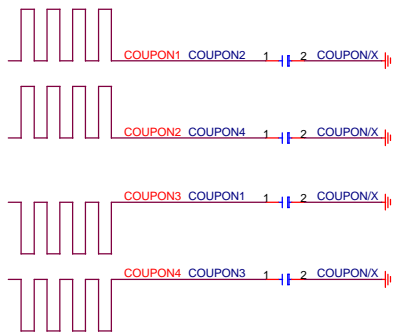
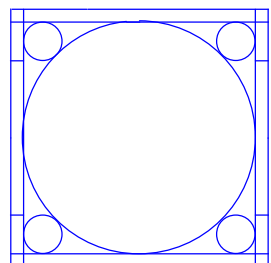
BLOCK DIAGRAM





HASWELL_E_EDS/LGA[10SC1-J02011-41R]

LGA2011-3 ILM_BP/2011/CSP12KRC-0F2011-61R]



CHANNEL A

LGA2011-3F HASWELL_E_EDS

M DA0	BU7	DDR0_DQ_0	DDR0_DQS_DP_0	BY6 M_DQSA0
M DA1	BT6	DDR0_DQ_1	DDR0_DQS_DN_0	BV6 M_-DQSA0
M DA2	CB8	DDR0_DQ_2		
M DA3	CB8	DDR0_DQ_3	DDR0_DQS_DP_1	BV12 M_DQSA1
M DA4	BT8	DDR0_DQ_4	DDR0_DQS_DN_1	BW11 M_-DQSA1
M DA5	BU8	DDR0_DQ_5		
M DA6	CA7	DDR0_DQ_6	DDR0_DQS_DP_2	CH10 M_DQSA2
M DA7	CB6	DDR0_DQ_7	DDR0_DQS_DN_2	CG11 M_-DQSA2
M DA8	BT12	DDR0_DQ_8		
M DA9	BU11	DDR0_DQ_9	DDR0_DQS_DP_3	CK14 M_DQSA3
M DA10	BW13	DDR0_DQ_10	DDR0_DQS_DN_3	CJ13 M_-DQSA3
M DA11	BY14	DDR0_DQ_11		
M DA12	BT14	DDR0_DQ_12	DDR0_DQS_DP_4	CK30 M_DQSA4
M DA13	BU15	DDR0_DQ_13	DDR0_DQS_DN_4	CM30 M_-DQSA4
M DA14	CA11	DDR0_DQ_14		
M DA15	BY12	DDR0_DQS_DP_5	DDR0_DQS_DP_5	CD30 M_DQSA5
M DA16	CE9	DDR0_DQ_16	DDR0_DQS_DN_5	CF30 M_-DQSA5
M DA17	CF8	DDR0_DQ_17		
M DA18	CK10	DDR0_DQ_18	DDR0_DQS_DP_6	CC37 M_DQSA6
M DA19	CI11	DDR0_DQ_19	DDR0_DQS_DN_6	CE37 M_-DQSA6
M DA20	CD10	DDR0_DQ_20		
M DA21	CE11	DDR0_DQ_21	DDR0_DQS_DP_7	CJ37 M_DQSA7
M DA22	CK8	DDR0_DQ_22	DDR0_DQS_DN_7	CL37 M_-DQSA7
M DA23	CJ8	DDR0_DQ_23		
M DA24	CE15	DDR0_DQ_24	DDR0_DQS_DP_8	CV10 M_DQSA8
M DA25	CG15	DDR0_DQ_25	DDR0_DQS_DN_8	CT10 M_-DQSA8
M DA26	CM14	DDR0_DQ_26		
M DA27	CH14	DDR0_DQ_27	DDR0_DQS_DP_9	BV8 M_DQSA9
M DA28	CC13	DDR0_DQ_28	DDR0_DQS_DN_9	BW9 M_-DQSA9
M DA29	CD14	DDR0_DQ_29		
M DA30	CM12	DDR0_DQ_30	DDR0_DQS_DP_10	BU13 M_DQSA10
M DA31	CI13	DDR0_DQ_31	DDR0_DQS_DN_10	BV14 M_-DQSA10
M DA32	CK28	DDR0_DQ_32		
M DA33	CH28	DDR0_DQ_33	DDR0_DQS_DP_11	CG9 M_DQSA11
M DA34	CK32	DDR0_DQ_34	DDR0_DQS_DN_11	CH8 M_-DQSA11
M DA35	CH32	DDR0_DQ_35		
M DA36	CI27	DDR0_DQ_36	DDR0_DQS_DP_12	CG13 M_DQSA12
M DA37	CJ27	DDR0_DQ_37	DDR0_DQS_DN_12	CE14 M_-DQSA12
M DA38	CI31	DDR0_DQ_38		
M DA39	CJ31	DDR0_DQ_39	DDR0_DQS_DP_13	CL29 M_DQSA13
M DA40	CD28	DDR0_DQ_40	DDR0_DQS_DN_13	CJ29 M_-DQSA13
M DA41	CB28	DDR0_DQ_41		
M DA42	CD32	DDR0_DQ_42	DDR0_DQS_DP_14	CE29 M_DQSA14
M DA43	CB32	DDR0_DQ_43	DDR0_DQS_DN_14	CC29 M_-DQSA14
M DA44	CE27	DDR0_DQ_44		
M DA45	CO27	DDR0_DQ_45	DDR0_DQS_DP_15	CE36 M_DQSA15
M DA46	CE31	DDR0_DQ_46	DDR0_DQS_DN_15	CD36 M_-DQSA15
M DA47	CC31	DDR0_DQ_47		
M DA48	CE35	DDR0_DQ_48	DDR0_DQS_DP_16	CM36 M_DQSA16
M DA49	CC35	DDR0_DQ_49	DDR0_DQS_DN_16	CK36 M_-DQSA16
M DA50	CE38	DDR0_DQ_50		
M DA51	CC39	DDR0_DQ_51	DDR0_DQS_DP_17	CU9 M_DQSA17
M DA52	CF34	DDR0_DQ_52	DDR0_DQS_DN_17	CW9 M_-DQSA17
M DA53	CD34	DDR0_DQ_53		
M DA54	CF38	DDR0_DQ_54		
M DA55	CD38	DDR0_DQ_55		
M DA56	CI38	DDR0_DQ_56		
M DA57	CJ35	DDR0_DQ_57		
M DA58	CI39	DDR0_DQ_58		
M DA59	CJ39	DDR0_DQ_59		
M DA60	CM34	DDR0_DQ_60		
M DA61	CK34	DDR0_DQ_61		
M DA62	CM38	DDR0_DQ_62		
M DA63	CK38	DDR0_DQ_63		
M AECC0	CT8	DDR0_ECC_0		
M AECC1	CV8	DDR0_ECC_1		
M AECC2	CW11	DDR0_ECC_2		
M AECC3	CU11	DDR0_ECC_3		
M AECC4	CP8	DDR0_ECC_4		
M AECC5	CN9	DDR0_ECC_5		
M AECC6	CB10	DDR0_ECC_6		
M AECC7	CR11	DDR0_ECC_7		

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CHANNEL B

LGA2011-3G HASWELL_E_EDS

M DB0	BV4	DDR1_DQ_0	DDR1_DQS_DP_0	BY4 M_DQSB0
M DB1	BU1	DDR1_DQ_1	DDR1_DQS_DN_0	BW3 M_-DQSB0
M DB2	CA3	DDR1_DQ_2		
M DB3	CB4	DDR1_DQ_3	DDR1_DQS_DP_1	CJ5 M_DQSB1
M DB4	BT4	DDR1_DQ_4	DDR1_DQS_DN_1	CH6 M_-DQSB1
M DB5	BT2	DDR1_DQ_5		
M DB6	CA1	DDR1_DQ_6	DDR1_DQS_DP_2	CT4 M_DQSB2
M DB7	BY2	DDR1_DQ_7	DDR1_DQS_DN_2	CV4 M_-DQSB2
M DB8	CE3	DDR1_DQ_8		
M DB9	CF4	DDR1_DQ_9	DDR1_DQS_DP_3	DB10 M_DQSB3
M DB10	CL5	DDR1_DQ_10	DDR1_DQS_DN_3	DC9 M_-DQSB3
M DB11	CM4	DDR1_DQ_11		
M DB12	CE5	DDR1_DQ_12	DDR1_DQS_DP_4	CT30 M_DQSB4
M DB13	CF6	DDR1_DQ_13	DDR1_DQS_DN_4	CV30 M_-DQSB4
M DB14	CK6	DDR1_DQ_14		
M DB15	CL3	DDR1_DQ_15	DDR1_DQS_DP_5	DD32 M_DQSB5
M DB16	CR3	DDR1_DQ_16	DDR1_DQS_DN_5	DB32 M_-DQSB5
M DB17	CV2	DDR1_DQ_17		
M DB18	CT6	DDR1_DQ_18	DDR1_DQS_DP_6	CR37 M_DQSB6
M DB19	CB6	DDR1_DQ_19	DDR1_DQS_DN_6	CJ37 M_-DQSB6
M DB20	CR1	DDR1_DQ_20		
M DB21	CP2	DDR1_DQ_21	DDR1_DQS_DP_7	DB38 M_DQSB7
M DB22	CU5	DDR1_DQ_22	DDR1_DQS_DN_7	DA37 M_-DQSB7
M DB23	CR5	DDR1_DQ_23		
M DB24	DA7	DDR1_DQ_24	DDR1_DQS_DP_8	DB14 M_DQSB8
M DB25	DB8	DDR1_DQ_25	DDR1_DQS_DN_8	DA13 M_-DQSB8
M DB26	DE11	DDR1_DQ_26		
M DB27	DC11	DDR1_DQ_27	DDR1_DQS_DP_9	BV2 M_DQSB9
M DB28	DA5	DDR1_DQ_28	DDR1_DQS_DN_9	BW1 M_-DQSB9
M DB29	CE6	DDR1_DQ_29		
M DB30	DE9	DDR1_DQ_30	DDR1_DQS_DP_10	CH4 M_DQSB10
M DB31	DE10	DDR1_DQ_31	DDR1_DQS_DN_10	CG3 M_-DQSB10
M DB32	CT28	DDR1_DQ_32		
M DB33	CP28	DDR1_DQ_33	DDR1_DQS_DP_11	CW3 M_DQSB11
M DB34	CT32	DDR1_DQ_34	DDR1_DQS_DN_11	CU3 M_-DQSB11
M DB35	CP32	DDR1_DQ_35		
M DB36	CU27	DDR1_DQ_36	DDR1_DQS_DP_12	DC7 M_DQSB12
M DB37	CR27	DDR1_DQ_37	DDR1_DQS_DN_12	DD8 M_-DQSB12
M DB38	CU31	DDR1_DQ_38		
M DB39	CR31	DDR1_DQ_39	DDR1_DQS_DP_13	CU29 M_DQSB13
M DB40	DA29	DDR1_DQ_40	DDR1_DQS_DN_13	CR29 M_-DQSB13
M DB41	DB30	DDR1_DQ_41		
M DB42	DC33	DDR1_DQ_42	DDR1_DQS_DP_14	DA31 M_DQSB14
M DB43	DE34	DDR1_DQ_43	DDR1_DQS_DN_14	CY32 M_-DQSB14
M DB44	DE28	DDR1_DQ_44		
M DB45	CY28	DDR1_DQ_45	DDR1_DQS_DP_15	CV36 M_DQSB15
M DB46	DA33	DDR1_DQ_46	DDR1_DQS_DN_15	CT36 M_-DQSB15
M DB47	DE33	DDR1_DQ_47		
M DB48	CU35	DDR1_DQ_48	DDR1_DQS_DP_16	DD36 M_DQSB16
M DB49	CR35	DDR1_DQ_49	DDR1_DQS_DN_16	DE37 M_-DQSB16
M DB50	CU39	DDR1_DQ_50		
M DB51	CR39	DDR1_DQ_51	DDR1_DQS_DP_17	CW13 M_DQSB17
M DB52	CV34	DDR1_DQ_52	DDR1_DQS_DN_17	CY14 M_-DQSB17
M DB53	CT34	DDR1_DQ_53		
M DB54	CV38	DDR1_DQ_54		
M DB55	CT39	DDR1_DQ_55		
M DB56	DC37	DDR1_DQ_56		
M DB57	DE36	DDR1_DQ_57		
M DB58	DC39	DDR1_DQ_58		
M DB59	DA39	DDR1_DQ_59		
M DB60	DC35	DDR1_DQ_60		
M DB61	DB36	DDR1_DQ_61		
M DB62	DE38	DDR1_DQ_62		
M DB63	DE39	DDR1_DQ_63		
M BECC0	CU13	DDR1_ECC_0		
M BECC1	CV14	DDR1_ECC_1		
M BECC2	DD14	DDR1_ECC_2		
M BECC3	DE14	DDR1_ECC_3		
M BECC4	CR13	DDR1_ECC_4		
M BECC5	CT14	DDR1_ECC_5		
M BECC6	DC13	DDR1_ECC_6		
M BECC7	DE13	DDR1_ECC_7		

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(11) M_DA[0..63] ↔ M_DA[0..63]
(11) M_DQSA[0..17] ↔ M_DQSA[0..17]
(11) M_-DQSA[0..17] ↔ M_-DQSA[0..17]
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Gigabyte Technology

Title		
CPU LGA2011-A		
Size	Document Number	Rev
Custom	GA-X99-UD5 WIFI	1.1
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CHANNEL C

LGA2011-3H HASWELL_E_EDS

M DC0	AD38	DDR2_DQ_0	DDR2_DQS_DP_0	V38	M -DQSC0
M DC1	AA37	DDR2_DQ_1	DDR2_DQS_DN_0	W37	M -DQSC0
M DC2	R37	DDR2_DQ_2			
M DC3	Y38	DDR2_DQ_3	DDR2_DQS_DP_1	U31	M -DQSC1
M DC4	AE37	DDR2_DQ_4	DDR2_DQS_DN_1	V32	M -DQSC1
M DC5	AC38	DDR2_DQ_5			
M DC6	T38	DDR2_DQ_6		AB32	M -DQSC2
M DC7	U37	DDR2_DQ_7	DDR2_DQS_DP_2	AD32	M -DQSC2
M DC8	V34	DDR2_DQ_8	DDR2_DQS_DN_2		
M DC9	U33	DDR2_DQ_9		U25	M -DQSC3
M DC10	V30	DDR2_DQ_10	DDR2_DQS_DP_3	W25	M -DQSC3
M DC11	T30	DDR2_DQ_11	DDR2_DQS_DN_3		
M DC12	U35	DDR2_DQ_12		N7	M -DQSC4
M DC13	R35	DDR2_DQ_13	DDR2_DQS_DP_4	P8	M -DQSC4
M DC14	T32	DDR2_DQ_14	DDR2_DQS_DN_4		
M DC15	W31	DDR2_DQ_15		AB10	M -DQSC5
M DC16	AD34	DDR2_DQ_16	DDR2_DQS_DP_5	Y10	M -DQSC5
M DC17	AB34	DDR2_DQ_17	DDR2_DQS_DN_5		
M DC18	AD30	DDR2_DQ_18		AH12	M -DQSC6
M DC19	AB30	DDR2_DQ_19	DDR2_DQS_DP_6	AJ13	M -DQSC6
M DC20	AC35	DDR2_DQ_20	DDR2_DQS_DN_6		
M DC21	AA35	DDR2_DQ_21		AJ7	M -DQSC7
M DC22	AE31	DDR2_DQ_22	DDR2_DQS_DP_7	AH8	M -DQSC7
M DC23	AC31	DDR2_DQ_23	DDR2_DQS_DN_7		
M DC24	U27	DDR2_DQ_24		AC25	M -DQSC8
M DC25	R27	DDR2_DQ_25	DDR2_DQS_DP_8	AE25	M -DQSC8
M DC26	U23	DDR2_DQ_26	DDR2_DQS_DN_8		
M DC27	R23	DDR2_DQ_27		AB38	M -DQSC9
M DC28	V28	DDR2_DQ_28	DDR2_DQS_DP_9	AC37	M -DQSC9
M DC29	T28	DDR2_DQ_29	DDR2_DQS_DN_9		
M DC30	V24	DDR2_DQ_30		T34	M -DQSC10
M DC31	T24	DDR2_DQ_31	DDR2_DQS_DP_10	R33	M -DQSC10
M DC32	N8	DDR2_DQ_32	DDR2_DQS_DN_10		
M DC33	K8	DDR2_DQ_33		AC33	M -DQSC11
M DC34	R7	DDR2_DQ_34	DDR2_DQS_DP_11	AA33	M -DQSC11
M DC35	P6	DDR2_DQ_35	DDR2_DQS_DN_11		
M DC36	J8	DDR2_DQ_36		V26	M -DQSC12
M DC37	L9	DDR2_DQ_37	DDR2_DQS_DP_12	T26	M -DQSC12
M DC38	KE	DDR2_DQ_38	DDR2_DQS_DN_12		
M DC39	M6	DDR2_DQ_39		M8	M -DQSC13
M DC40	U8	DDR2_DQ_40	DDR2_DQS_DP_13	L7	M -DQSC13
M DC41	W11	DDR2_DQ_41	DDR2_DQS_DN_13		
M DC42	AA11	DDR2_DQ_42		V8	M -DQSC14
M DC43	AB8	DDR2_DQ_43	DDR2_DQS_DP_14	W9	M -DQSC14
M DC44	T10	DDR2_DQ_44	DDR2_DQS_DN_14		
M DC45	U11	DDR2_DQ_45		AH16	M -DQSC15
M DC46	AA9	DDR2_DQ_46	DDR2_DQS_DP_15	AJ15	M -DQSC15
M DC47	Y8	DDR2_DQ_47	DDR2_DQS_DN_15		
M DC48	AE11	DDR2_DQ_48		AH10	M -DQSC16
M DC49	AE12	DDR2_DQ_49	DDR2_DQS_DP_16	AJ9	M -DQSC16
M DC50	AK12	DDR2_DQ_50	DDR2_DQS_DN_16		
M DC51	AL13	DDR2_DQ_51		AD26	M -DQSC17
M DC52	AG15	DDR2_DQ_52	DDR2_DQS_DP_17	AB26	M -DQSC17
M DC53	AF14	DDR2_DQ_53	DDR2_DQS_DN_17		
M DC54	AK14	DDR2_DQ_54			
M DC55	AL15	DDR2_DQ_55			
M DC56	AG9	DDR2_DQ_56			
M DC57	AG7	DDR2_DQ_57			
M DC58	AK10	DDR2_DQ_58			
M DC59	AL9	DDR2_DQ_59			
M DC60	AE7	DDR2_DQ_60			
M DC61	AE9	DDR2_DQ_61			
M DC62	AK8	DDR2_DQ_62			
M DC63	AL7	DDR2_DQ_63			
M CECC0	AC27	DDR2_ECC_0			
M CECC1	AA27	DDR2_ECC_1			
M CECC2	AC23	DDR2_ECC_2			
M CECC3	AA23	DDR2_ECC_3			
M CECC4	AD28	DDR2_ECC_4			
M CECC5	AB28	DDR2_ECC_5			
M CECC6	AD24	DDR2_ECC_6			
M CECC7	AB24	DDR2_ECC_7			

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(13) M_DC[0..63] <=> M_DC[0..63]

(13) M_DQSC[0..17] <=> M_DQSC[0..17]

(13) M_-DQSC[0..17] <=> M_-DQSC[0..17]

(13) M_CECC[0..7] <=> M_CECC[0..7]

CHANNEL D

LGA2011-3I HASWELL_E_EDS

M DD0	D38	DDR3_DQ_0	DDR3_DQS_DP_0	E37	M -DQSD0
M DD1	B38	DDR3_DQ_1	DDR3_DQS_DN_0	C37	M -DQSD0
M DD2	L37	DDR3_DQ_2			
M DD3	M38	DDR3_DQ_3	DDR3_DQS_DP_1	B32	M -DQSD1
M DD4	C39	DDR3_DQ_4	DDR3_DQS_DN_1	A33	M -DQSD1
M DD5	J39	DDR3_DQ_5			
M DD6	G37	DDR3_DQ_6		M32	M -DQSD2
M DD7	K38	DDR3_DQ_7	DDR3_DQS_DP_2	K32	M -DQSD2
M DD8	A35	DDR3_DQ_8	DDR3_DQS_DN_2		
M DD9	B34	DDR3_DQ_9		E25	M -DQSD3
M DD10	G31	DDR3_DQ_10	DDR3_DQS_DP_3	G25	M -DQSD3
M DD11	E31	DDR3_DQ_11	DDR3_DQS_DN_3		
M DD12	F34	DDR3_DQ_12		H2	M -DQSD4
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M DD14	D32	DDR3_DQ_14	DDR3_DQS_DN_4		
M DD15	E33	DDR3_DQ_15		E7	M -DQSD5
M DD16	K34	DDR3_DQ_16	DDR3_DQS_DP_5	C7	M -DQSD5
M DD17	M34	DDR3_DQ_17	DDR3_DQS_DN_5		
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M DD19	M30	DDR3_DQ_19	DDR3_DQS_DP_6	AJ1	M -DQSD6
M DD20	J35	DDR3_DQ_20	DDR3_DQS_DN_6		
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M DD22	L31	DDR3_DQ_22	DDR3_DQS_DP_7	AA5	M -DQSD7
M DD23	N31	DDR3_DQ_23	DDR3_DQS_DN_7		
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M DD26	F24	DDR3_DQ_26	DDR3_DQS_DN_8		
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M DD28	G29	DDR3_DQ_28	DDR3_DQS_DP_9	H38	M -DQSD9
M DD29	F29	DDR3_DQ_29	DDR3_DQS_DN_9		
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M DD32	K4	DDR3_DQ_32	DDR3_DQS_DN_10		
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M DD34	J1	DDR3_DQ_34	DDR3_DQS_DP_11	L33	M -DQSD11
M DD35	L1	DDR3_DQ_35	DDR3_DQS_DN_11		
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M DD37	N3	DDR3_DQ_37	DDR3_DQS_DP_12	D26	M -DQSD12
M DD38	K2	DDR3_DQ_38	DDR3_DQS_DN_12		
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M DD40	E9	DDR3_DQ_40	DDR3_DQS_DP_13	L3	M -DQSD13
M DD41	F8	DDR3_DQ_41	DDR3_DQS_DN_13		
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M DD47	G7	DDR3_DQ_47	DDR3_DQS_DN_15		
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M DD49	AG1	DDR3_DQ_49	DDR3_DQS_DP_16	W5	M -DQSD16
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M DD58	AC5	DDR3_DQ_58			
M DD59	AE5	DDR3_DQ_59			
M DD60	U5	DDR3_DQ_60			
M DD61	V6	DDR3_DQ_61			
M DD62	AC3	DDR3_DQ_62			
M DD63	AB6	DDR3_DQ_63			
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M DECC5	M28	DDR3_ECC_5			
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9 OF 19

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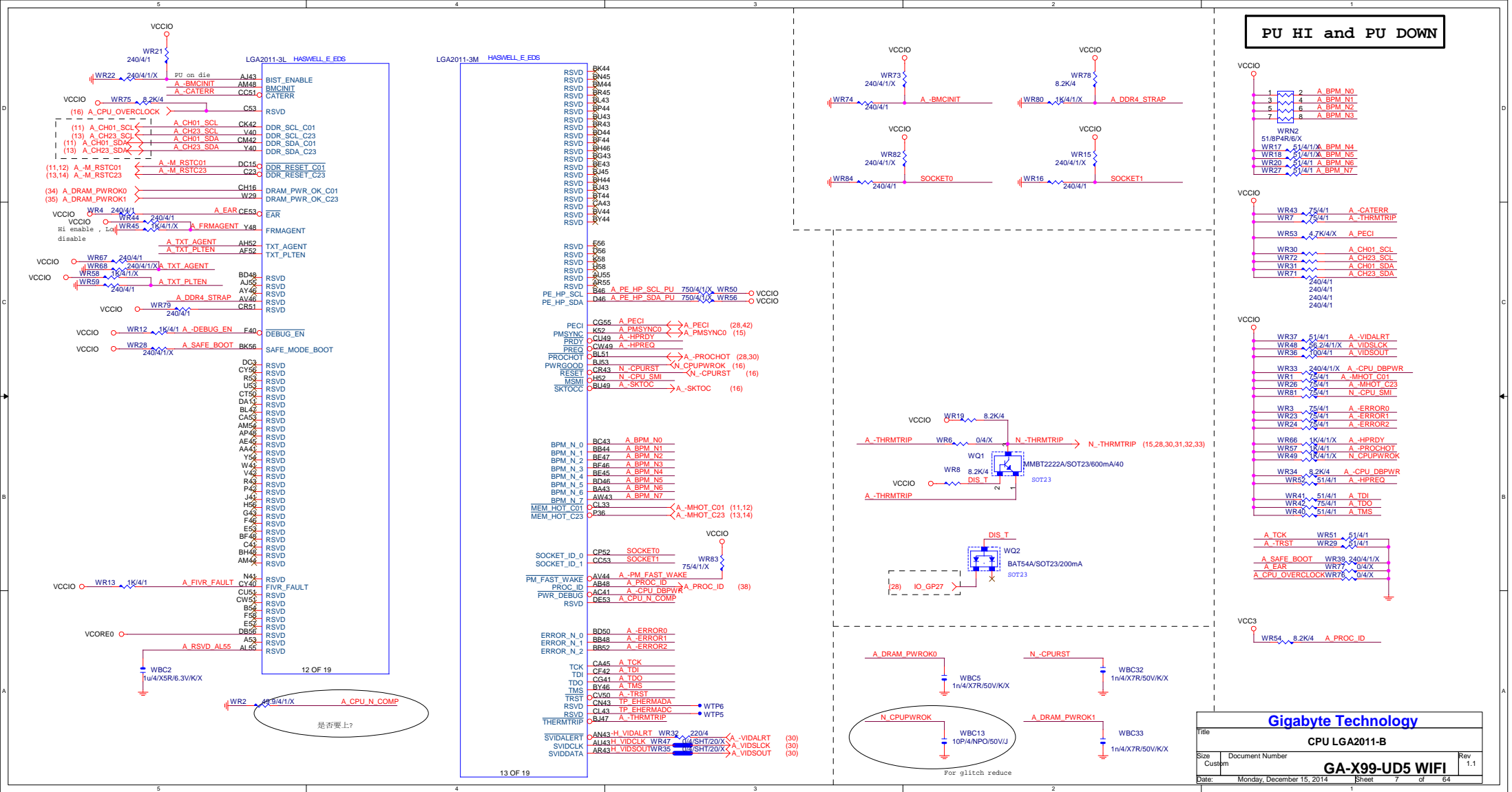
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Gigabyte Technology

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Size			Document Number		
Custom			GA-X99-UD5 WIFI		
Date:			Monday, December 15, 2014		
			Sheet 6 of 64		
			Rev 1.1		

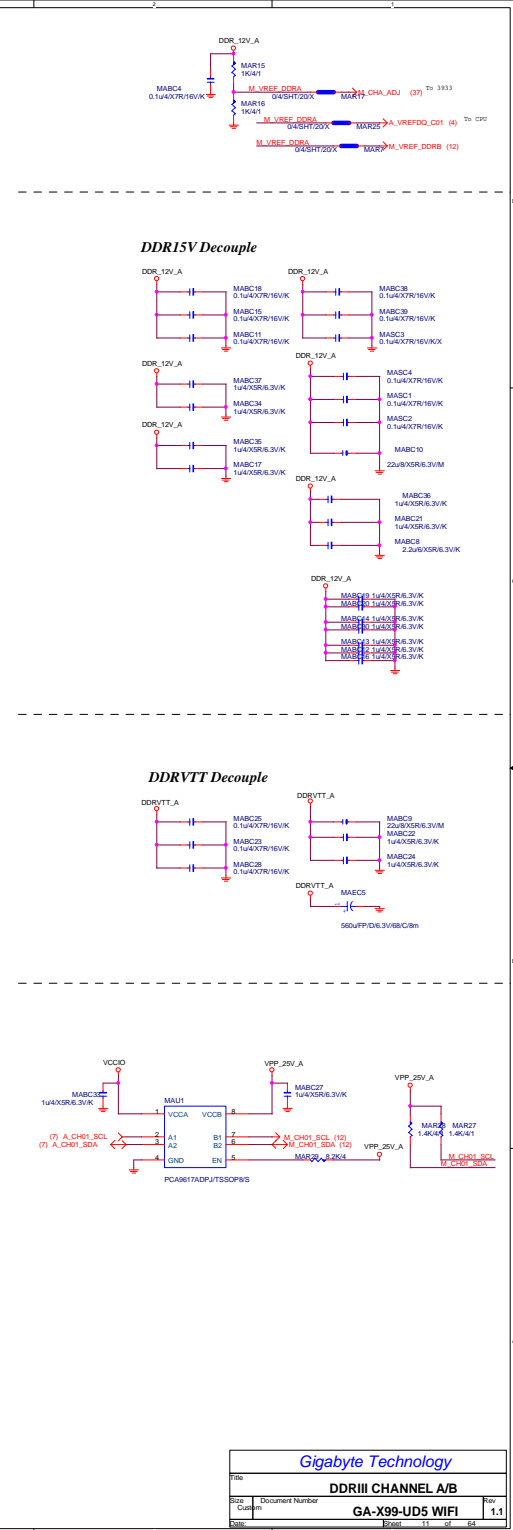


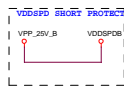
Gigabyte Technology			
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Size Custom	Document Number GA-X99-UD5 WIFI		Rev 1.1
Date:	Monday, December 15, 2014		Sheet 8 of 64

LGA2011-3P

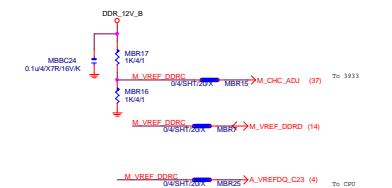
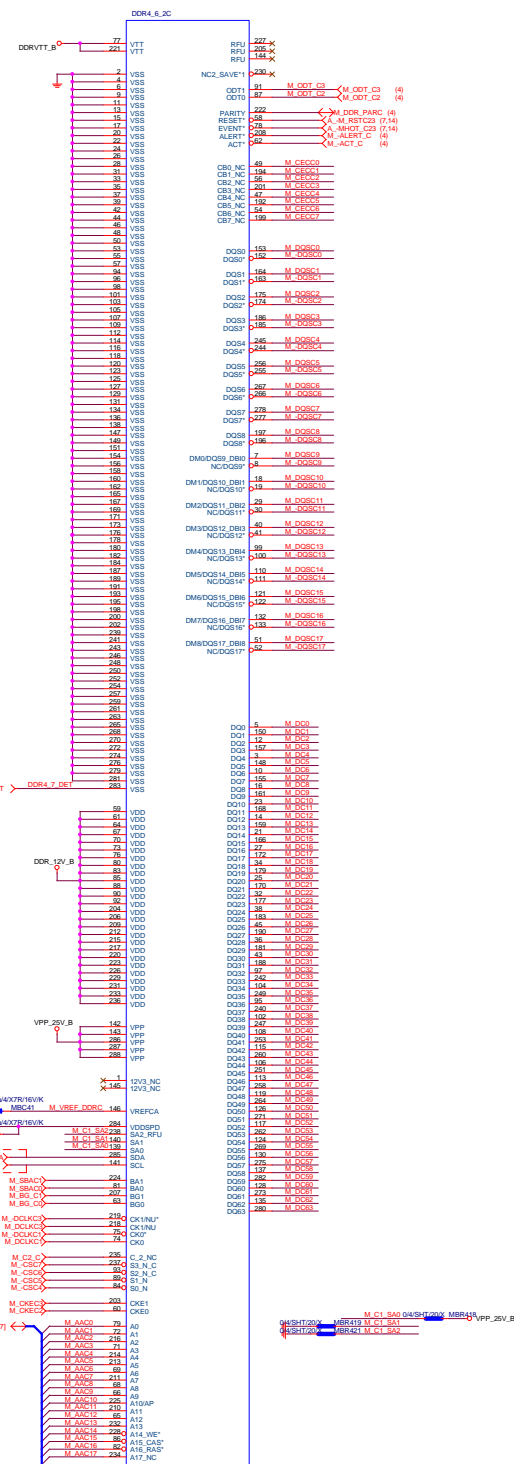
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CC45	VSS	CB42
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CC41	VSS	CB38
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CC33	VSS	CB30
CC31	VSS	CB28
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CC25	VSS	CB22
CC23	VSS	CB20
CC21	VSS	CB18
CC19	VSS	CB16
CC17	VSS	CB14
CC15	VSS	CB12
CC13	VSS	CB10
CC11	VSS	CB8
CC9	VSS	CB6
CC7	VSS	CB4
CC5	VSS	CB2
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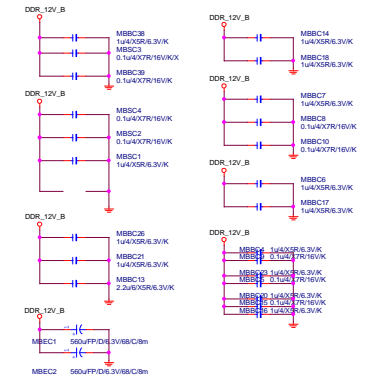




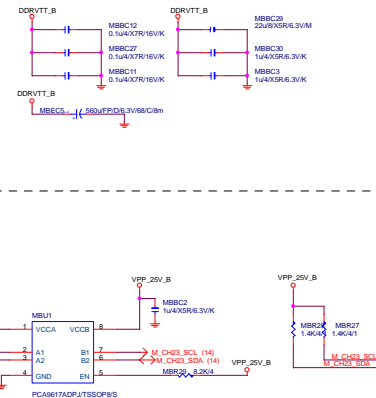
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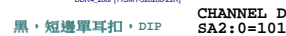
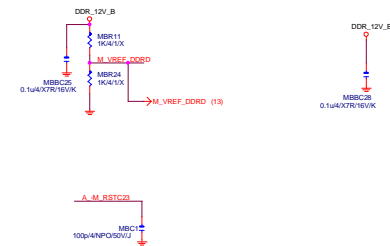


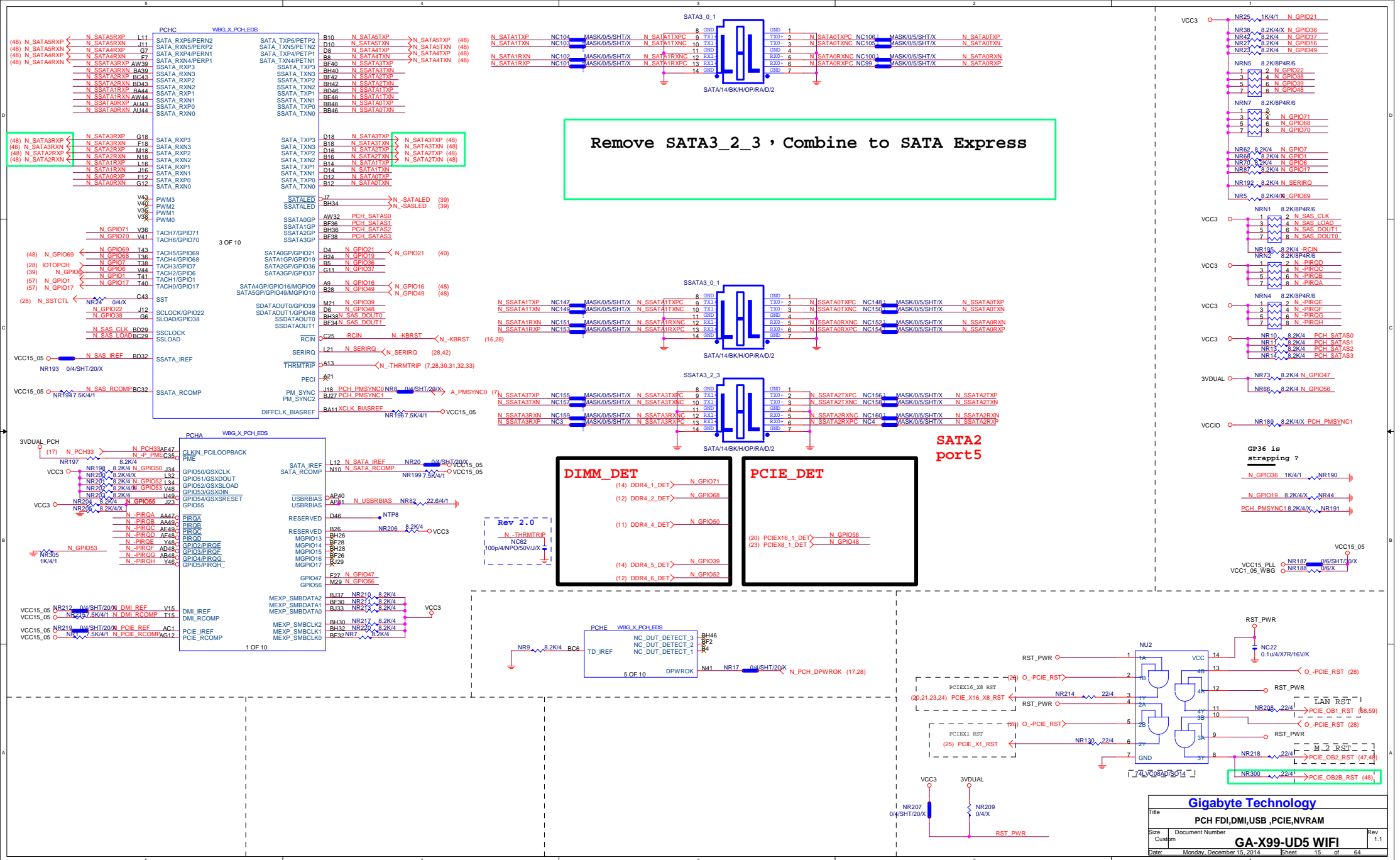
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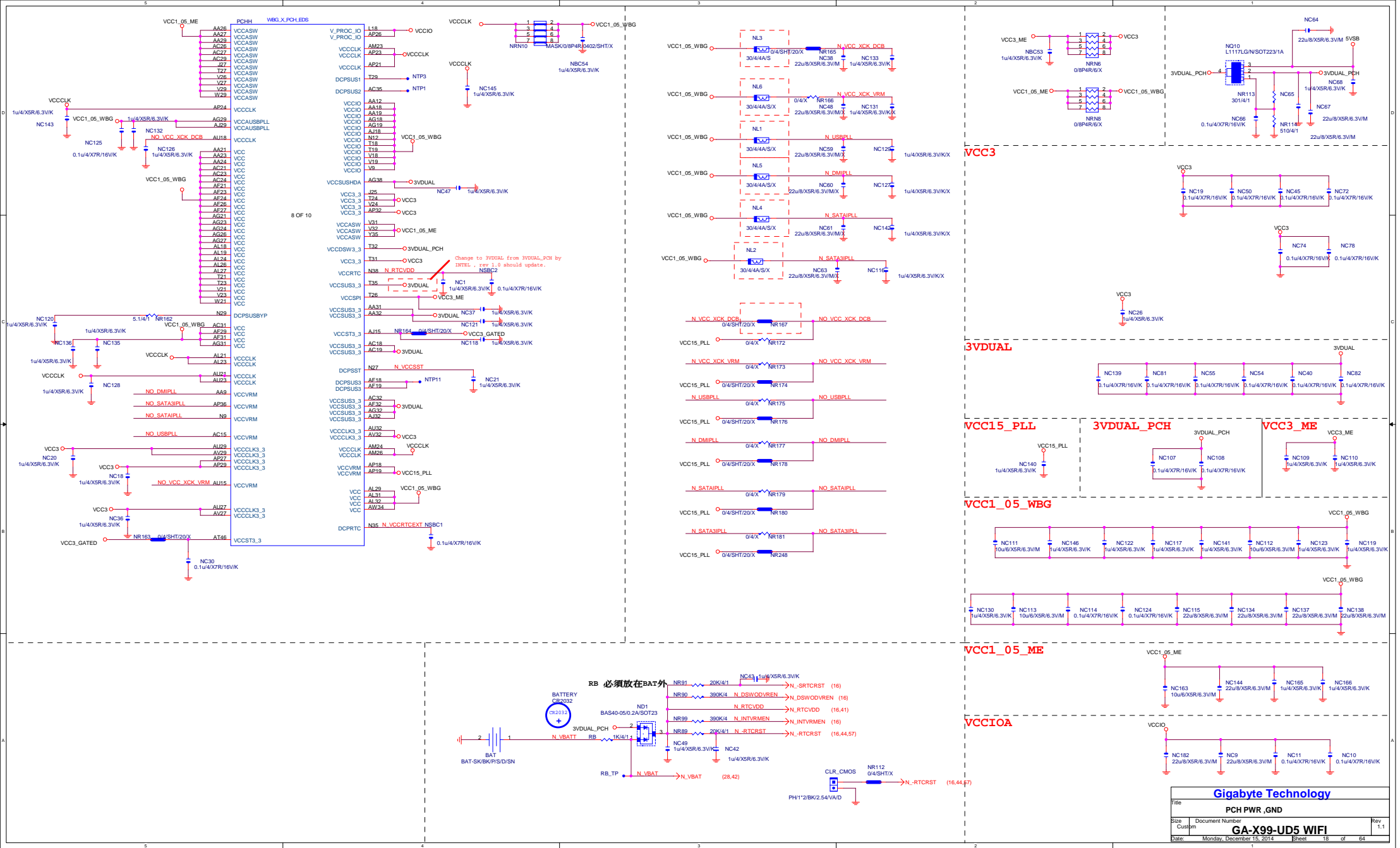


DDRVTT Decouple









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AU14	VSS	BD18
AU3	VSS	BD20
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AU36	VSS	BD27
AU38	VSS	BD30
AU40	VSS	BD34
AU41	VSS	BD36
AU49	VSS	BD39
AU9	VSS	BD41
AV18	VSS	BD44
AV20	VSS	BD6
AV21	VSS	BD9
AV23	VSS	BF18
AV25	VSS	BF4
AV30	VSS	BF44
AW1	VSS	BF46
AW16	VSS	BF48
AW18	VSS	BG11
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AW29	VSS	BG17
AW3	VSS	BG19
AW38	VSS	BG21
AW43	VSS	BG23
AW47	VSS	BG25
AW49	VSS	BG27
B22	VSS	BG29
BA1	VSS	BG31
BA14	VSS	BG33
BA16	VSS	BG35
BA20	VSS	BG37
BA21	VSS	BG39
BA25	VSS	BG41
BA27	VSS	BG43
BA29	VSS	BG7
BA3	VSS	BG9
BA30	VSS	BH18
BA32	VSS	BH4
BA36	VSS	B111
BA38	VSS	B113
BA41	VSS	B115
BA43	VSS	B119
BA47	VSS	B123
BA49	VSS	B125
BA9	VSS	B131
BC12	VSS	B135
BC27	VSS	B139
BC3	VSS	B141
A13	VSS	B143
AJ31	VSS	B17
AJ38	VSS	B19
A16	VSS	C11
A17	VSS	C13
A19	VSS	C15
AK12	VSS	C17
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AK35	VSS	AM38
AK38	VSS	AM9
AK41	VSS	AN1
AK44	VSS	AN3
AK46	VSS	AP10
AK6	VSS	AP15
AK9	VSS	AP31
AL1	VSS	AP35
AL3	VSS	AP38
AL49	VSS	AP46
AM14	VSS	AP6
AM15	VSS	AR1
AM18	VSS	AR3
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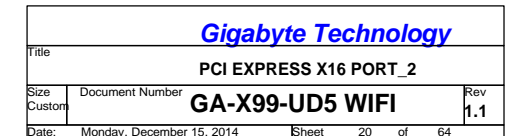
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AA44	VSS	A27
AB46	VSS	A29
AC10	VSS	A31
AC3	VSS	A35
AC49	VSS	A39
AC6	VSS	A43
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AD19	VSS	C23
AD21	VSS	C7
AD23	VSS	C9
AD24	VSS	D22
AD26	VSS	D24
AD27	VSS	D28
AD29	VSS	D32
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AD32	VSS	D40
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AE15	VSS	F16
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AE35	VSS	F23
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AE41	VSS	F30
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AE6	VSS	F41
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AF46	VSS	F9
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AG3	VSS	G3
AG47	VSS	G49
AG49	VSS	J1
AH48	VSS	J14
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AJ12	VSS	J30
AJ14	VSS	J36
AJ19	VSS	J41
AJ21	VSS	J9
AJ23	VSS	K46
AJ24	VSS	L1
AJ26	VSS	Y12
L3	VSS	Y15
L49	VSS	Y38
L7	VSS	Y41
M20	VSS	Y44
M25	VSS	Y6
M30	VSS	Y9
M32	VSS	U1
N1	VSS	U3
N3	VSS	U47
N32	VSS	V14
P12	VSS	V46
P15	VSS	W1
P35	VSS	W18
P38	VSS	W19
P41	VSS	W23
P44	VSS	W24
P46	VSS	W26
P6	VSS	W27
P9	VSS	W3
R1	VSS	W31
R3	VSS	W32
R49	VSS	W47
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AU47	VSS	T48
	VSS	T6
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A46	VSS	BH48
A48	VSS	BH49
A5	VSS	B12
A7	VSS	B14
B2	VSS	B146
B48	VSS	B148
B49	VSS	B15
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BF1	VSS	E1
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BH1	VSS	

Gigabyte Technology

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Size	Document Number	Rev	
Custom	GA-X99-UD5 WIFI	1.1	
Date:	Monday, December 15, 2014	Sheet	19 of 64

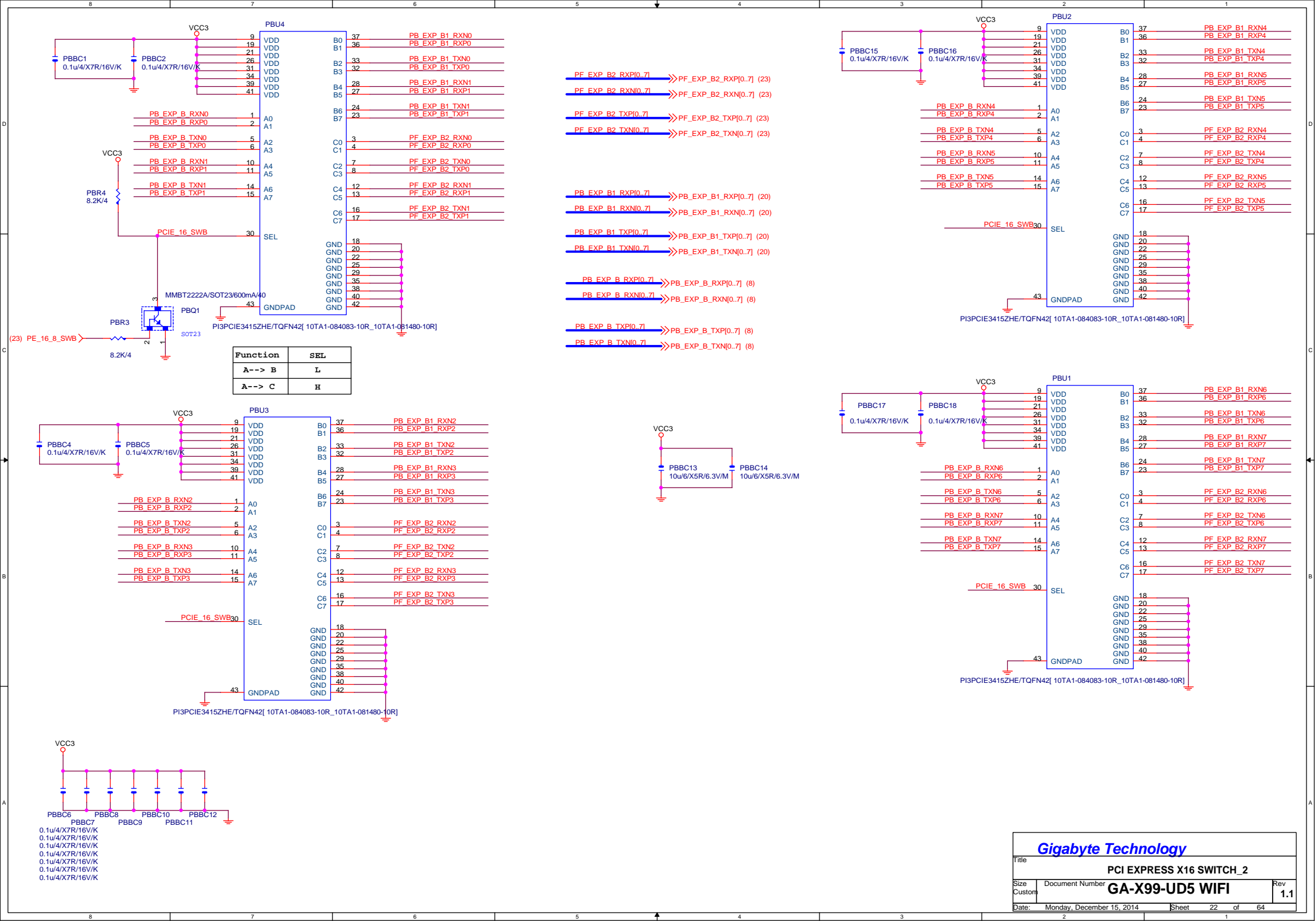
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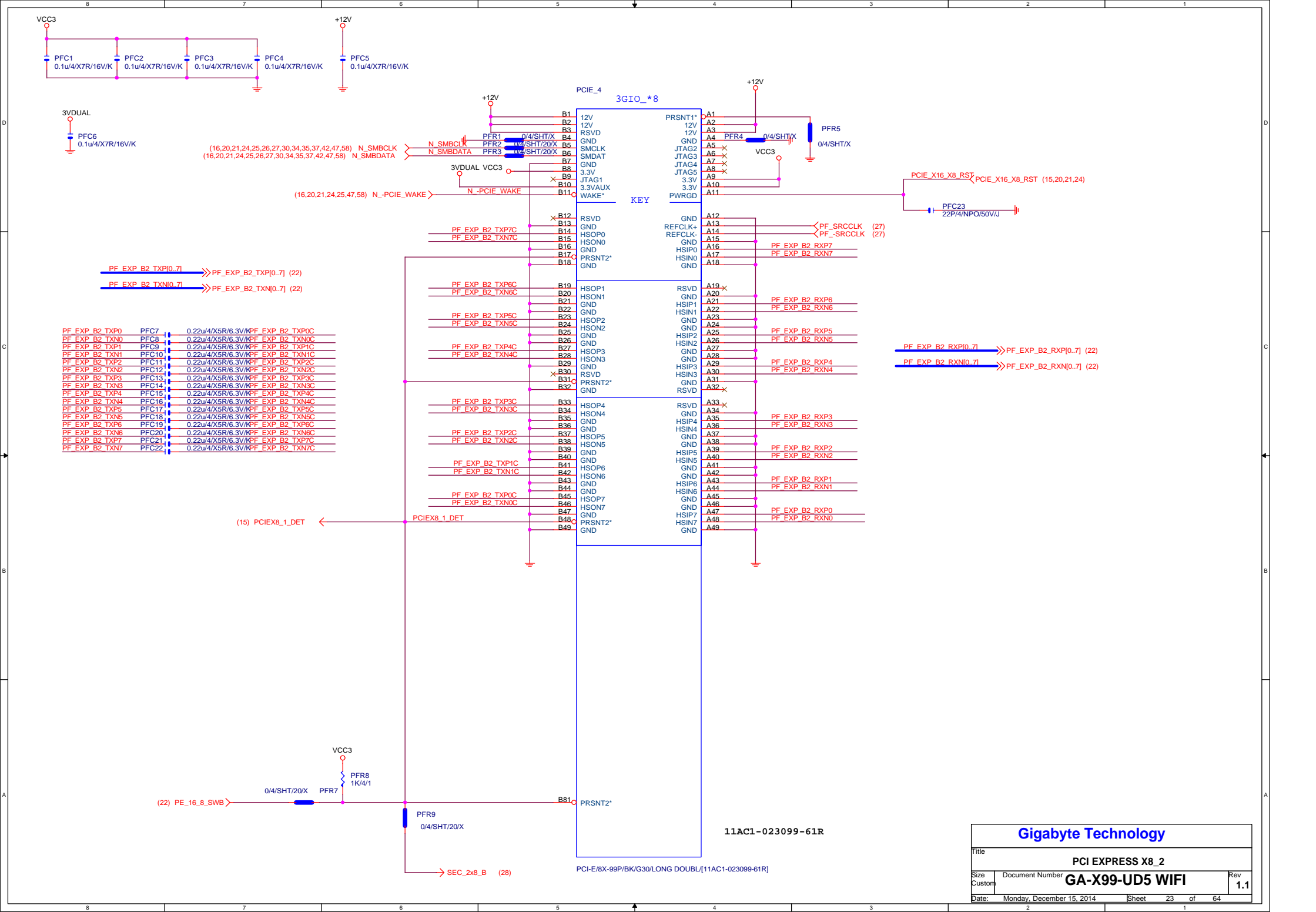


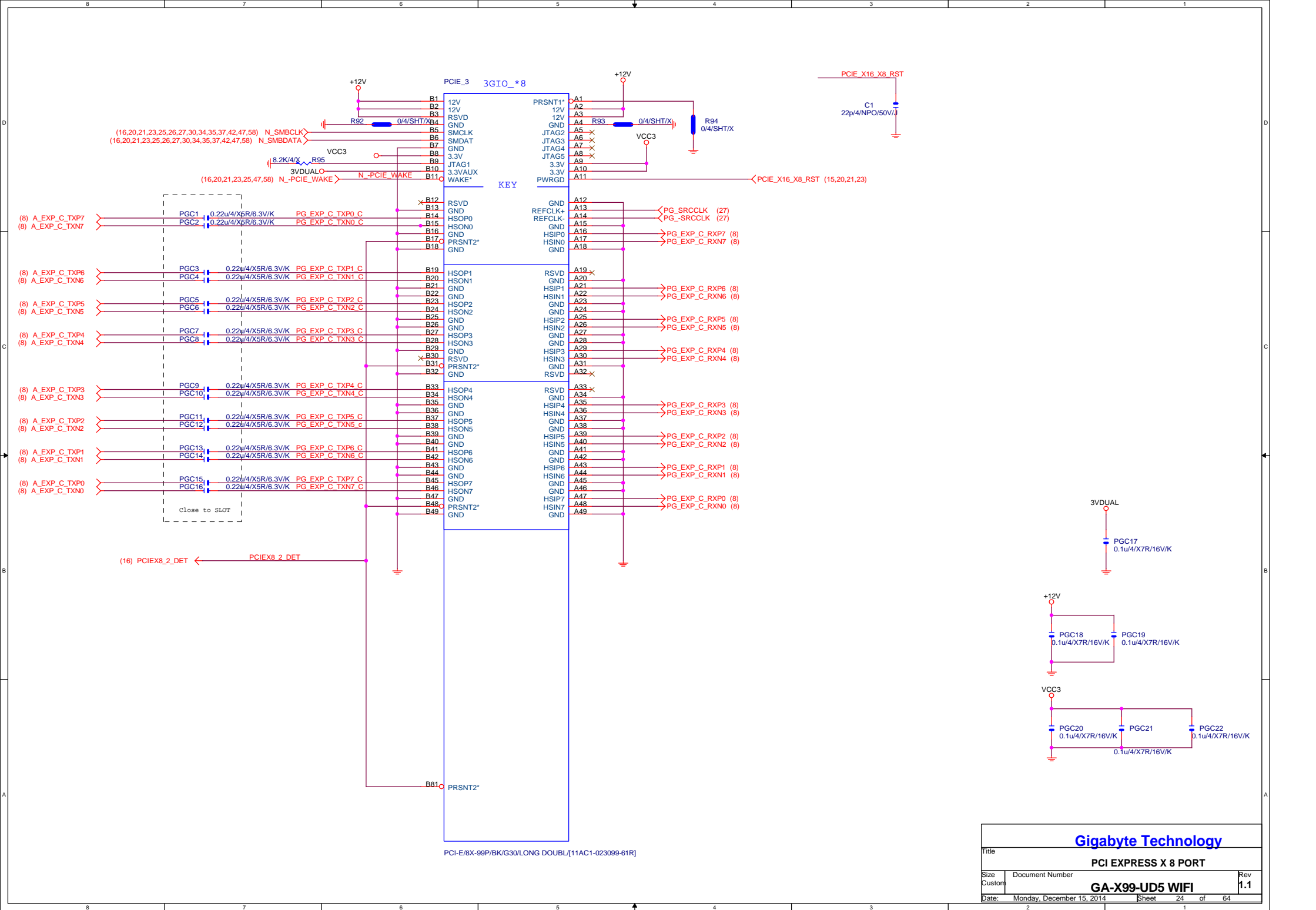
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PCIE_2 3GIO_*16



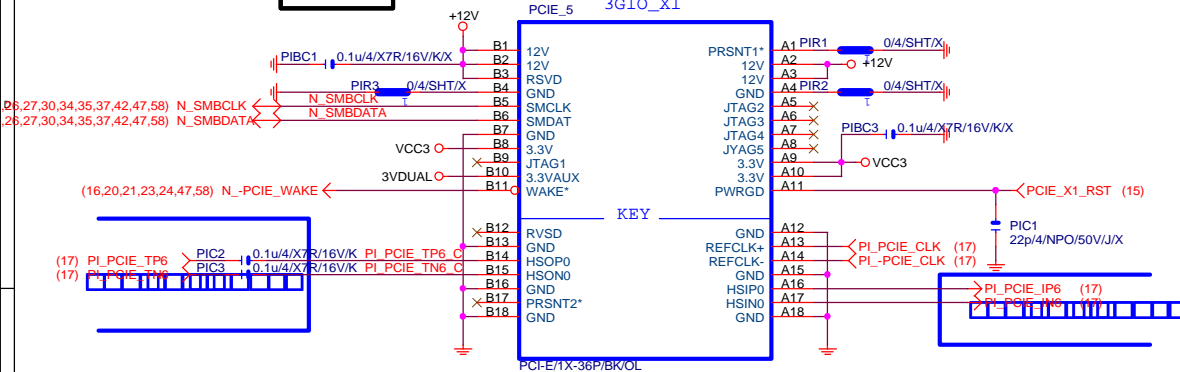




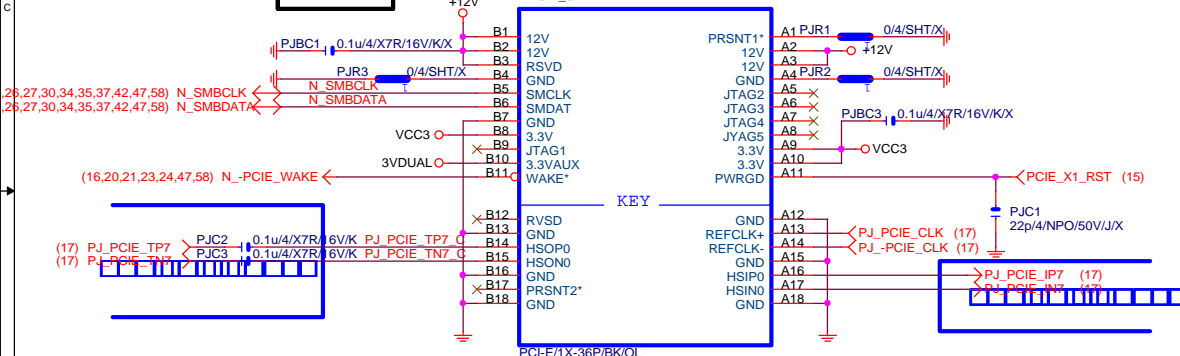


PCIEX1 SLOT

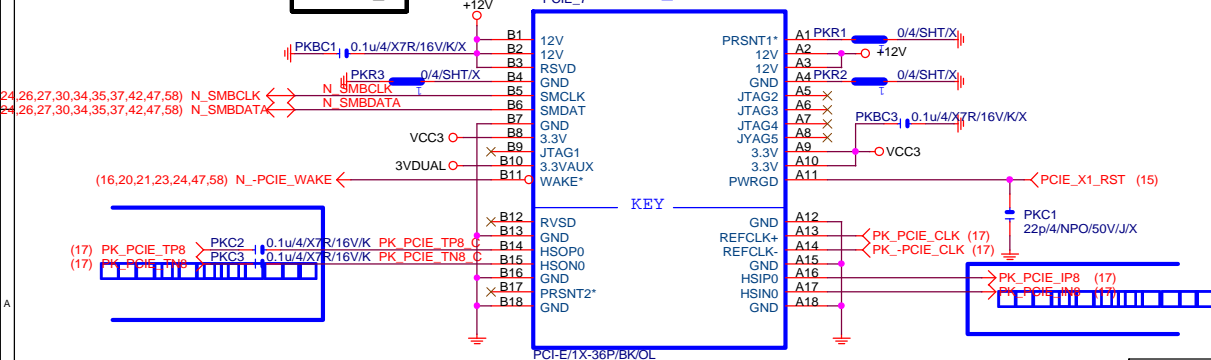
PCIEX1_1



PCIEX1_2

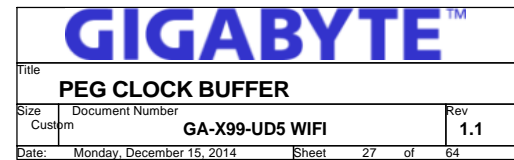
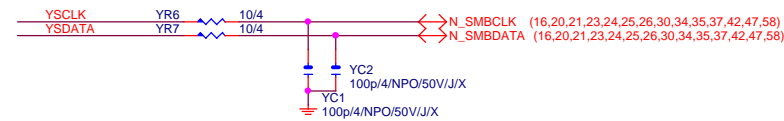
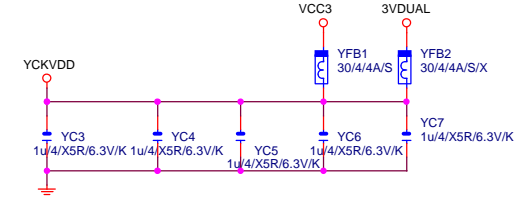
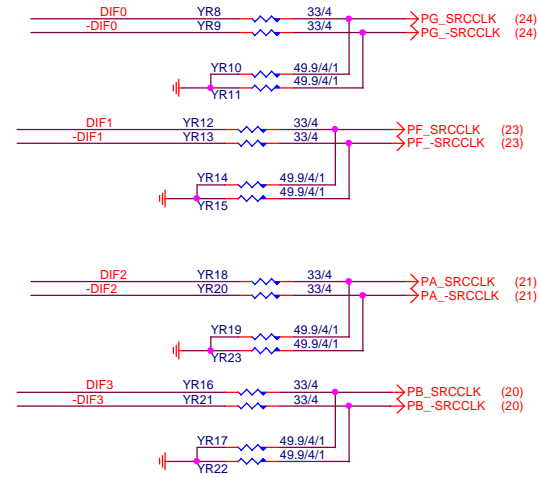
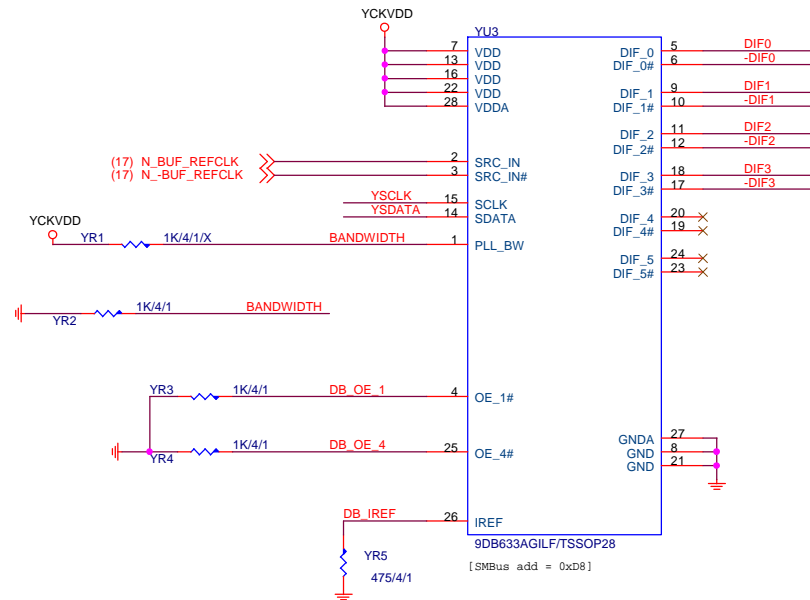
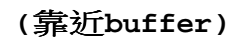


PCIEX1_3



Gigabyte Technology

Title			PCIE_X1 1,2,3
Size	Document Number	GA-X99-UD5 WIFI	
Custom		Rev	1.1
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JP2
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OR80
1K/4/1

ITE PWROK2
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OR177
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OR2
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OR4
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OR17
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OR129
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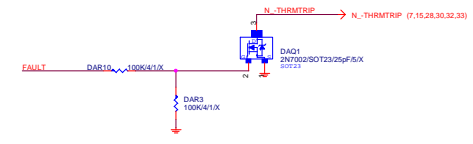
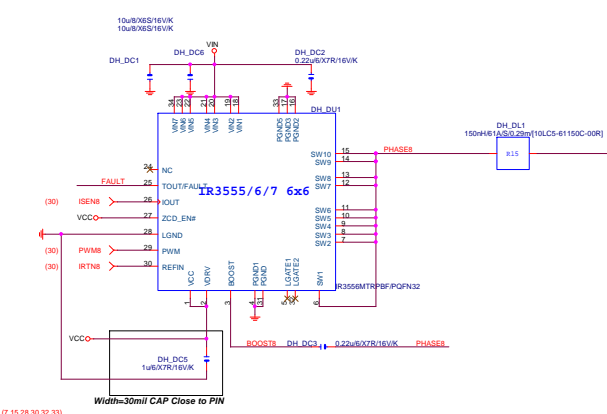
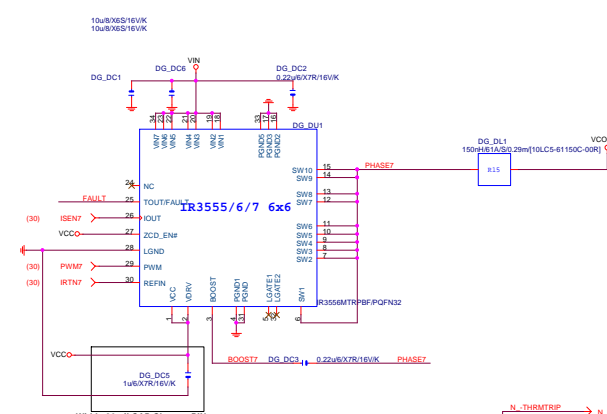
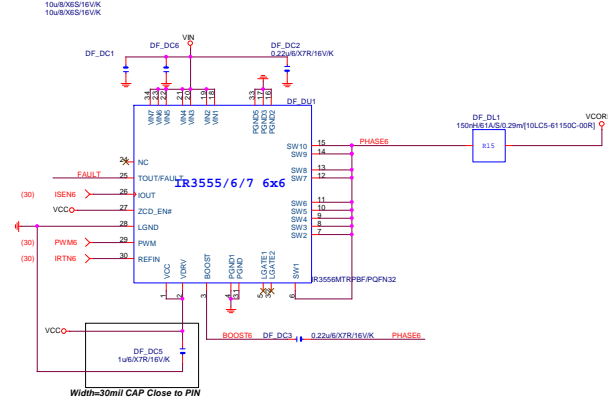
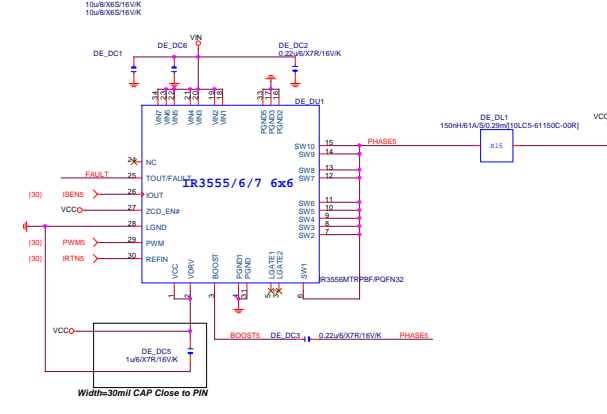
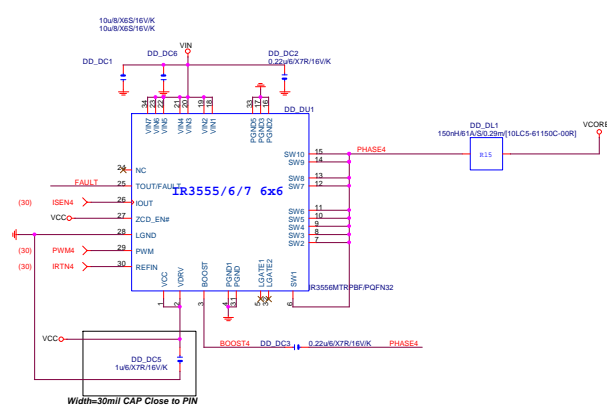
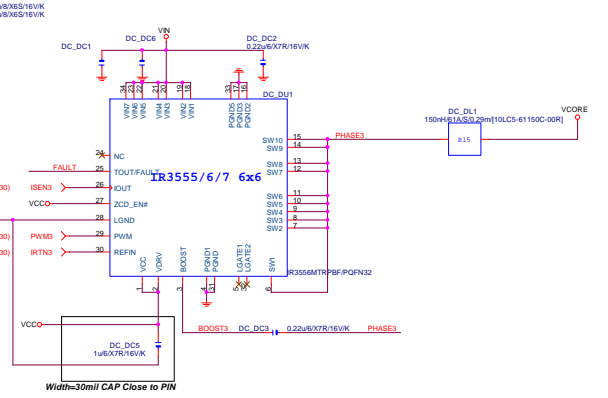
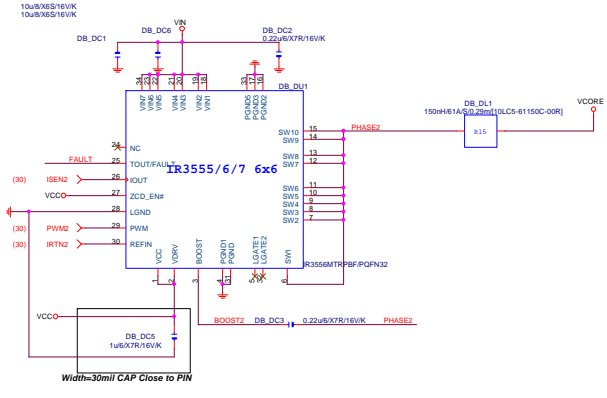
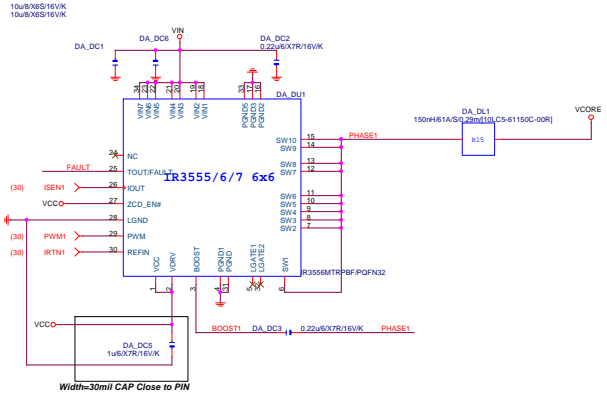
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DDR_A(3553)



DDR_B

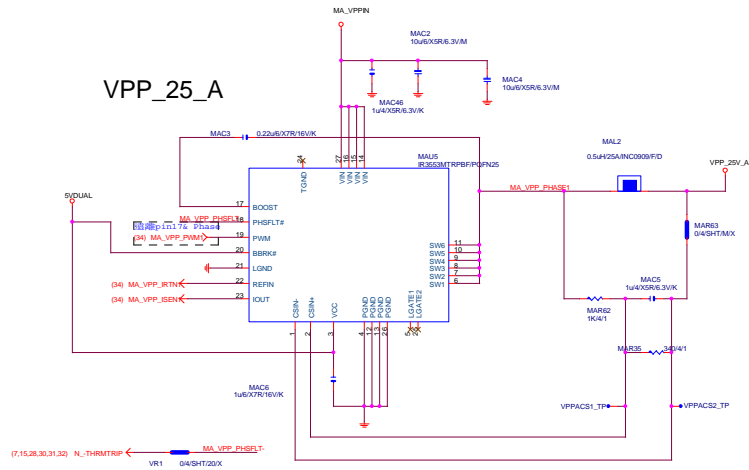
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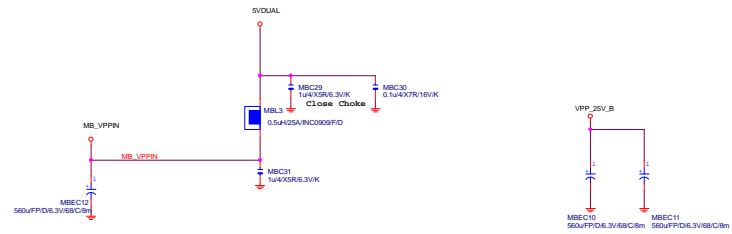
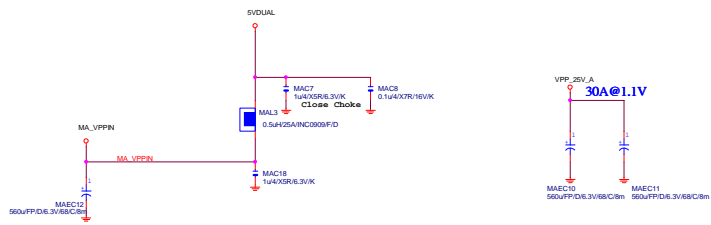
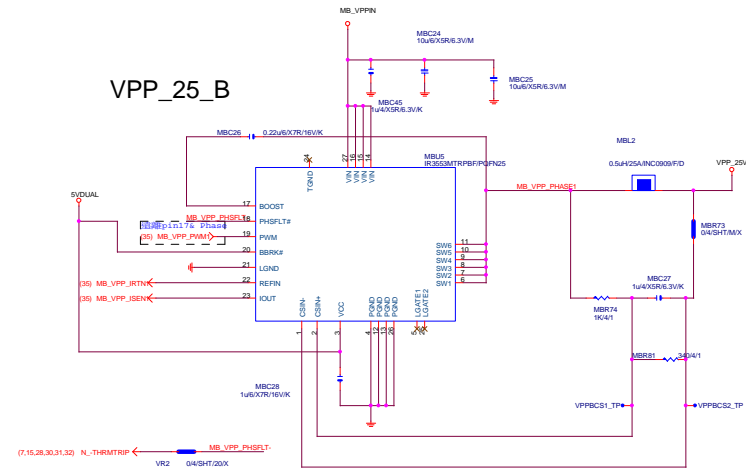
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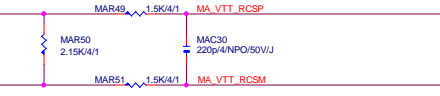
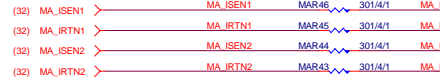
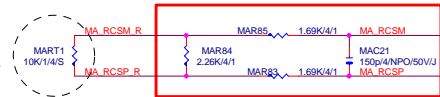
VPP_25_A



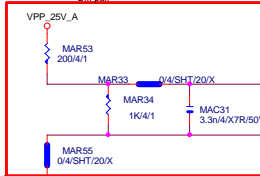
VPP_25_B



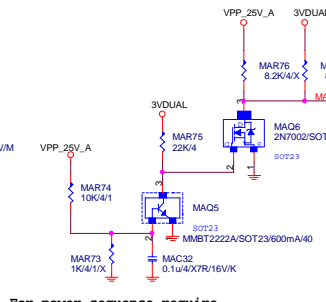
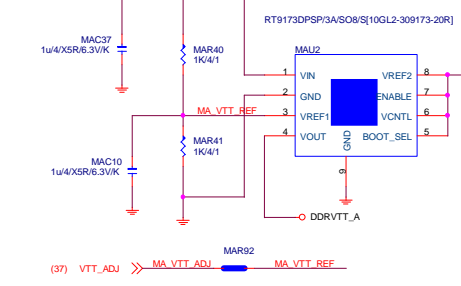
Close to Vcore
output inductor



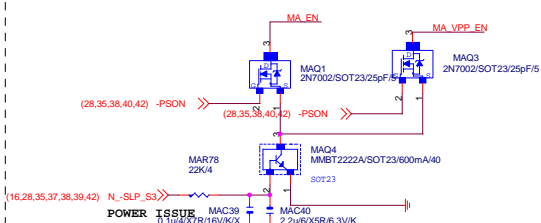
should be routed as
differential pair,
7mil width, 8mil
spacing



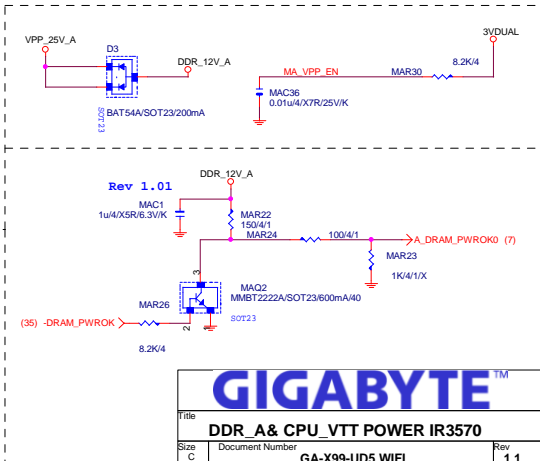
DDRVTT



For power sequence require



POWER ISSUE



GIGABYTE™			
DDR_A & CPU_VTT POWER IR3570			
Size	Document Number	Rev	
C	GA-X99-UD5 WIFI	1.1	
Date:	Monday, December 15, 2014	Sheet	34 of 64

Close to Vcore
output inductor

should be routed as
differential pair,
7mil width,8mil
spacing

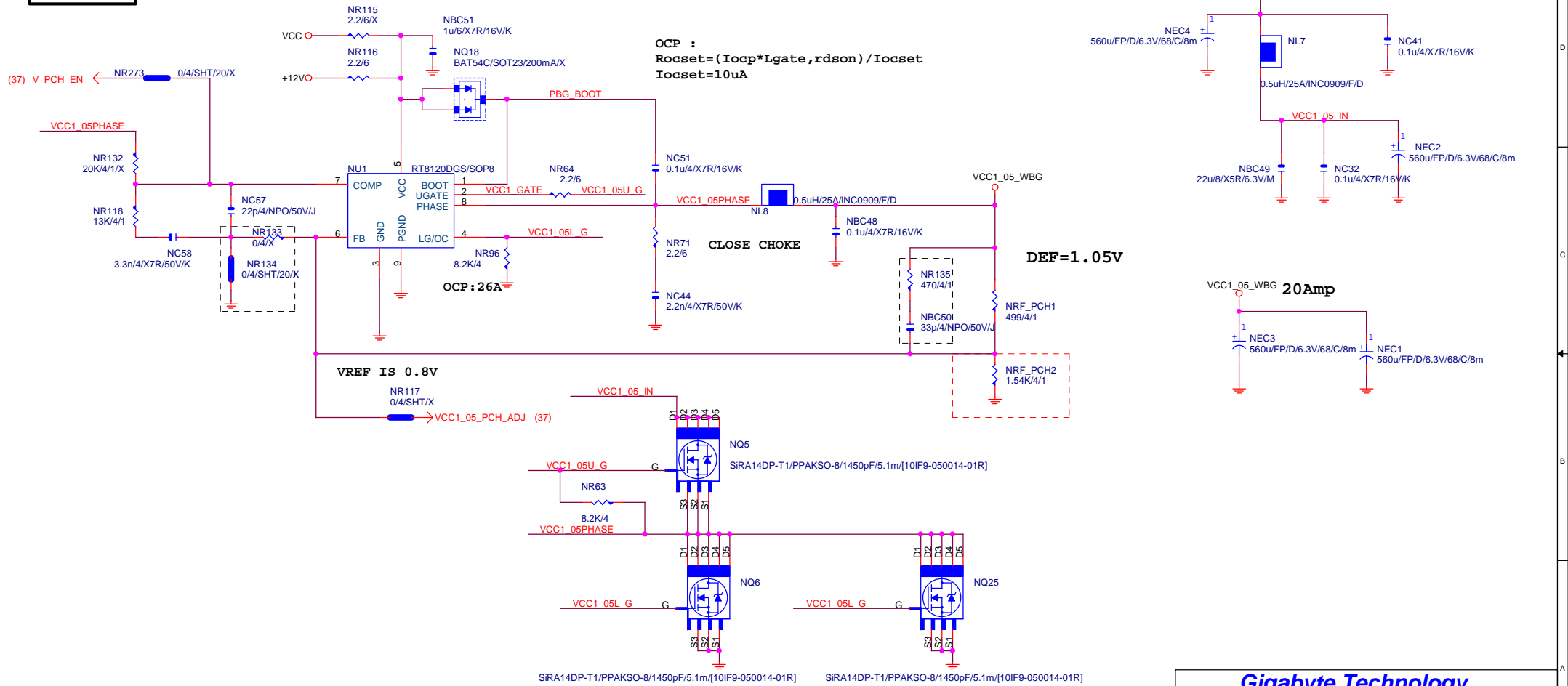
For power sequence require

POWER ISUE
0.1u4/X7R/16V/K

GIGABYTE

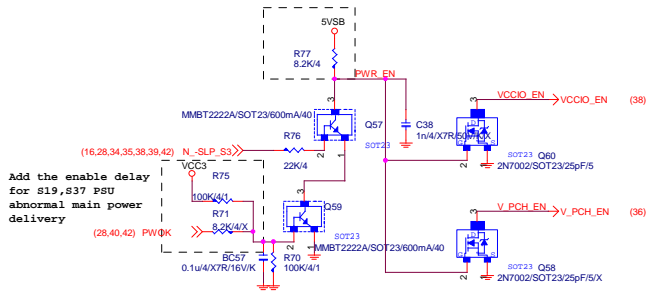
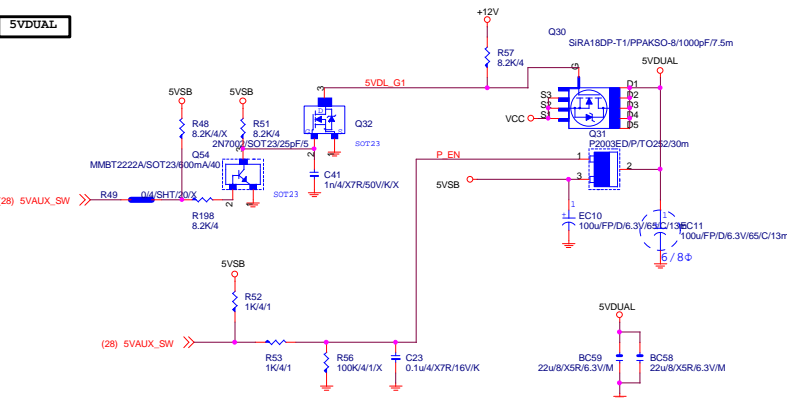
Title			DDR_A & CPU_VTT POWER IR3570
Size	Document Number	GA-X99-UD5 WIFI	
C		Rev	1.1
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PBG_1.1V



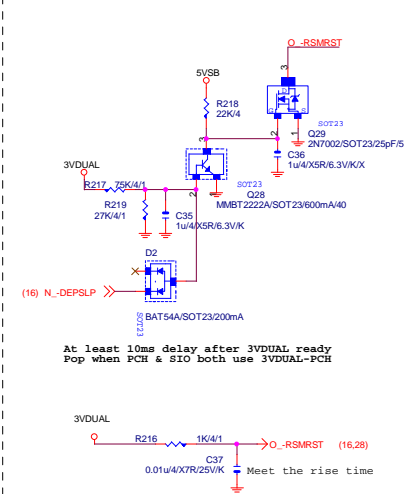
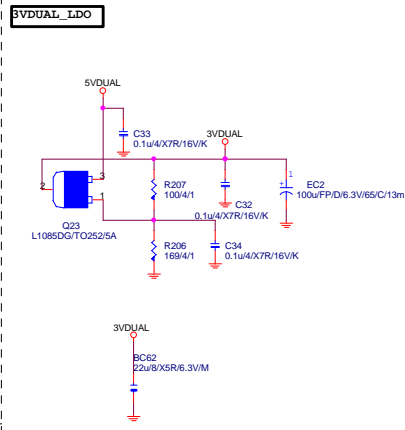
Gigabyte Technology			
Title			
RT8120 PCH			
Size	Document Number		Rev
Custom	GA-X99-UD5 WIFI		1.1
Date:	Monday, December 15, 2014	Sheet	36 of 64

5VDUAL



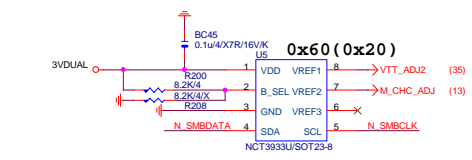
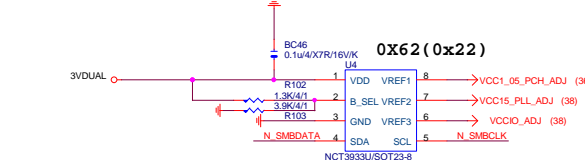
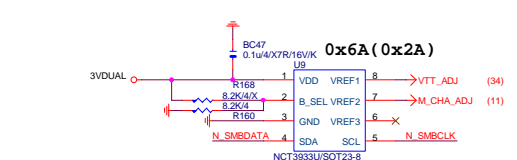
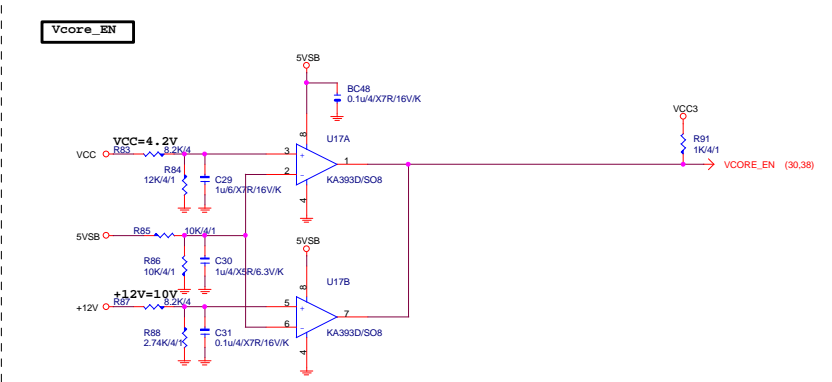
Add the enable delay for #19, #37 P8U abnormal main power delivery

3VDUAL_LDO

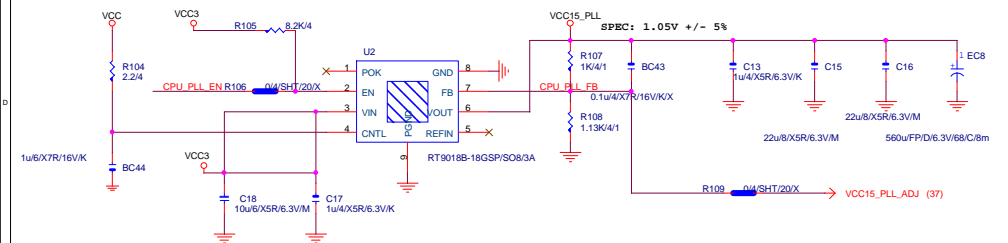


At least 10ms delay after 3VDUAL ready Pop when PCH & SIO both use 3VDUAL-PCH

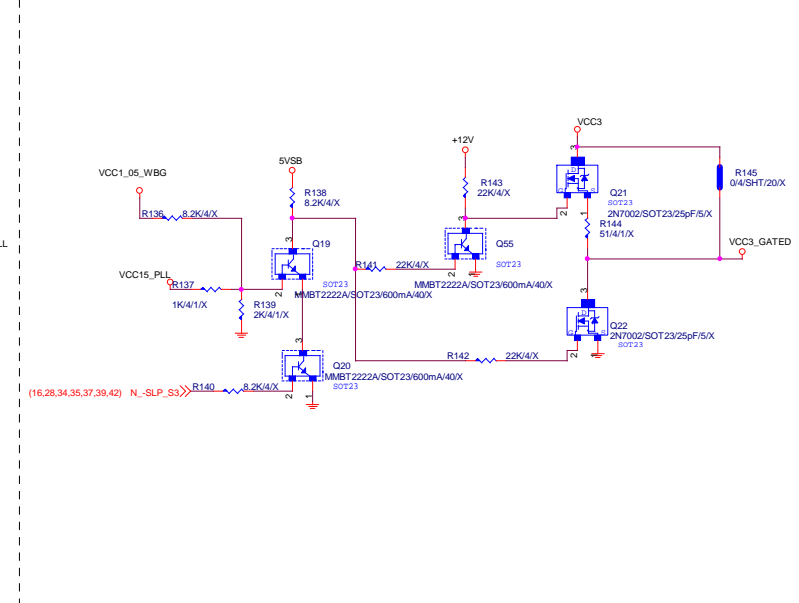
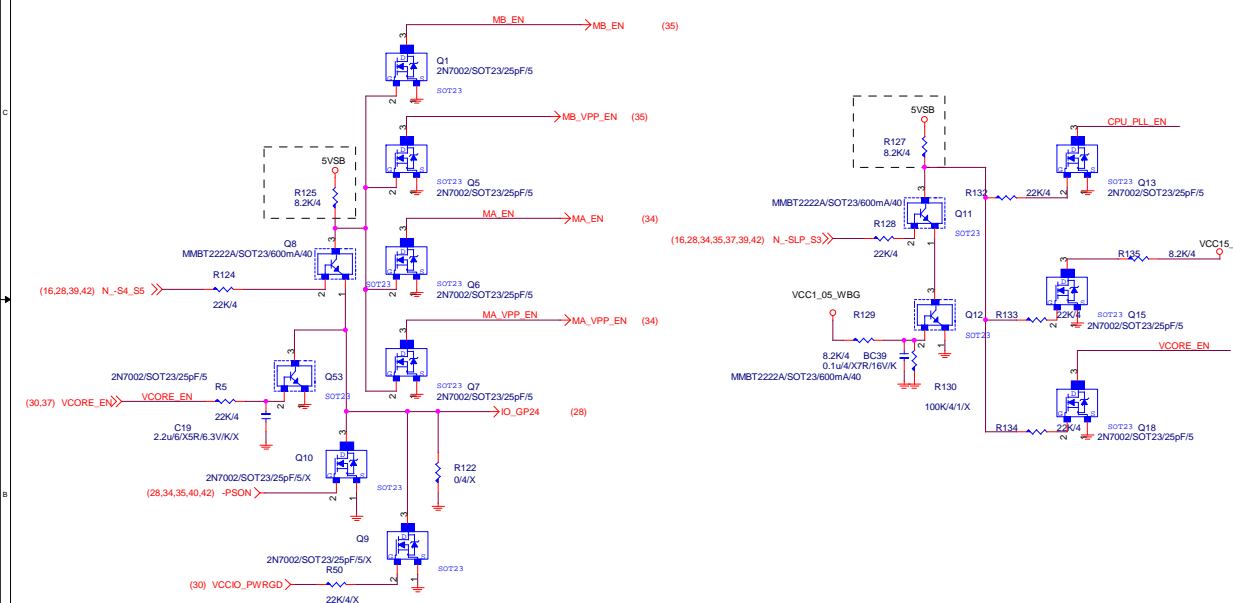
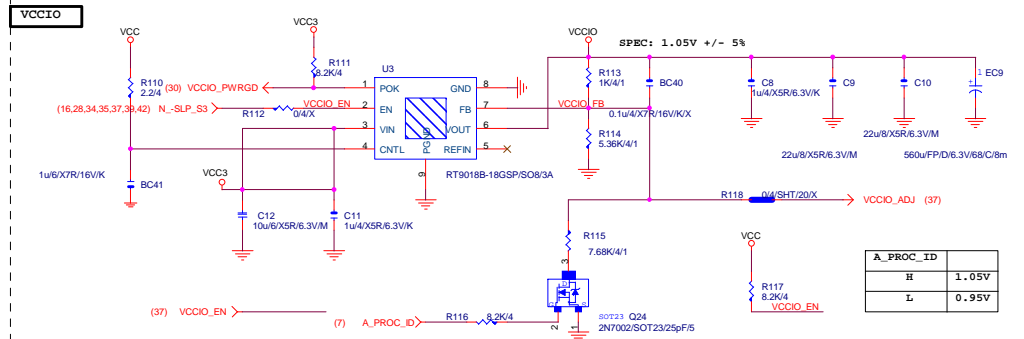
Vcore_EN



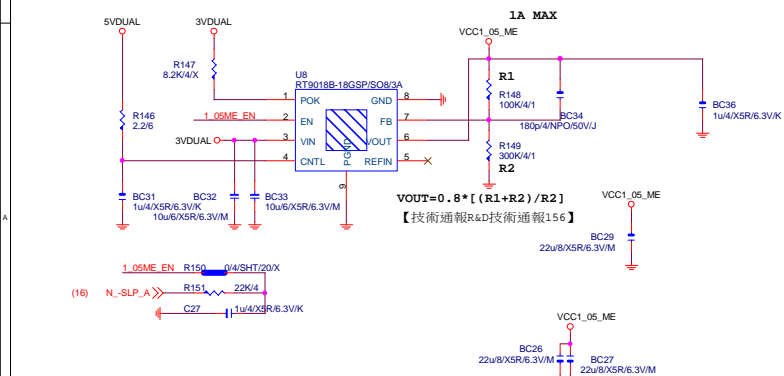
VCC15_PLL



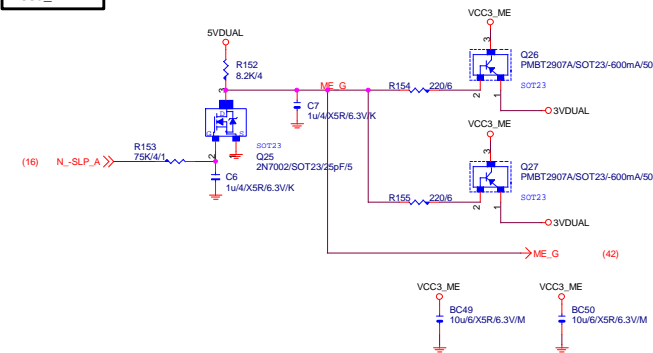
VCCIO



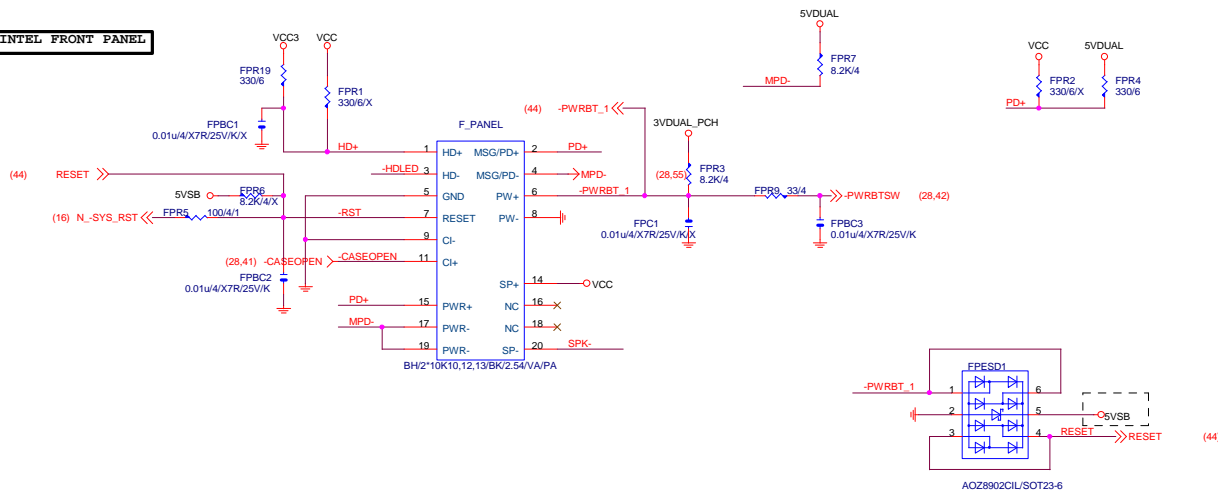
VCC1 05 ME



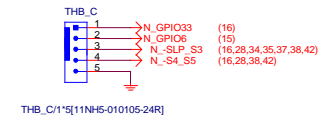
VCC3 ME



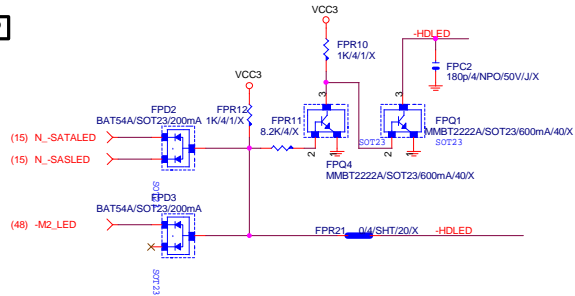
INTEL FRONT PANEL



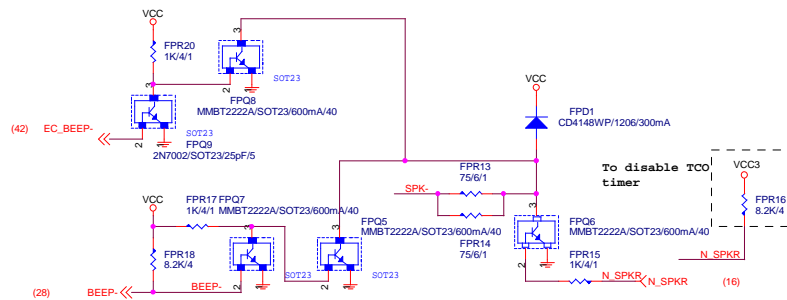
Thunderbolt



SATA LED

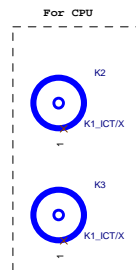
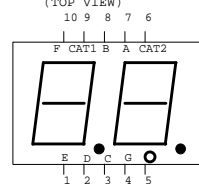
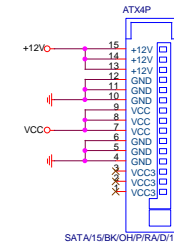
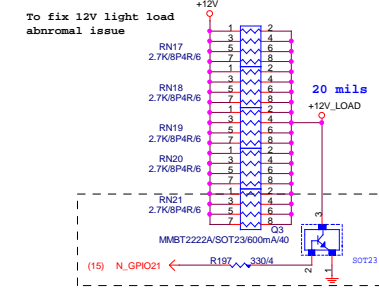


SPKR

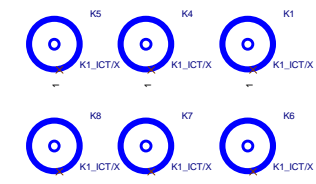


Gigabyte Technology			
Title	FP,TPM THB		
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Custom		Rev	1.1
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OVER CLOCKING



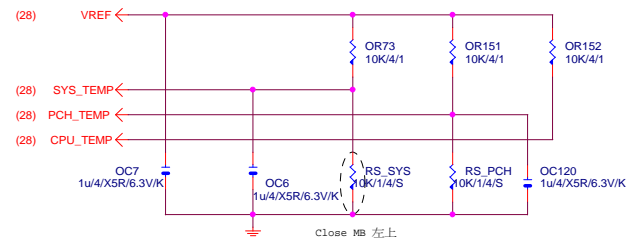
INPUT				OUTPUT	
PR	CL	CLOCK	DATA	Q	-Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	Rising	H	H	L
L	H	Rising	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	Falling	X	No Change	

Gigabyte Technology

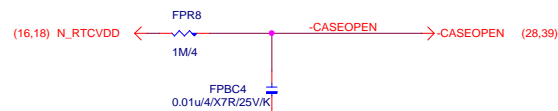
Title	ATX , 80PORT
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Size C	Document Number GA-X99-UD5 WIFI	Rev 1.1
Date:	Monday, December 15, 2014	Sheet 40 of 64

TEMP H/W MONITOR

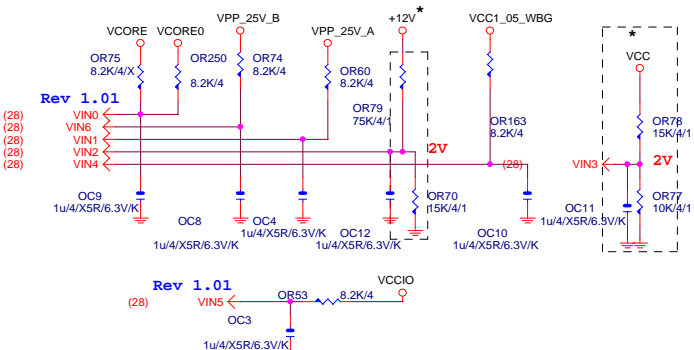


CASE OPEN

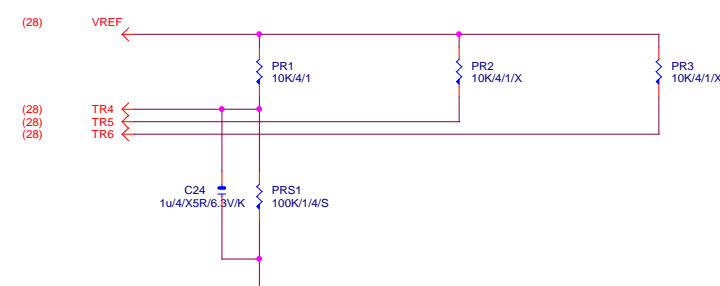


VOLTAGE-- H/W MONITOR

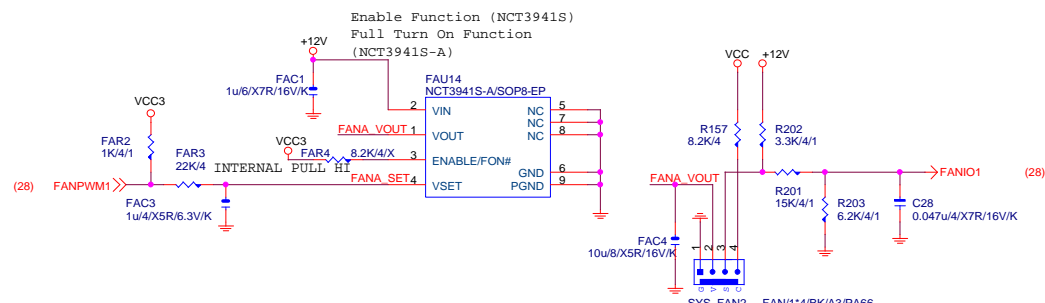
VIN2 must +12V input
VIN3 must VCC input



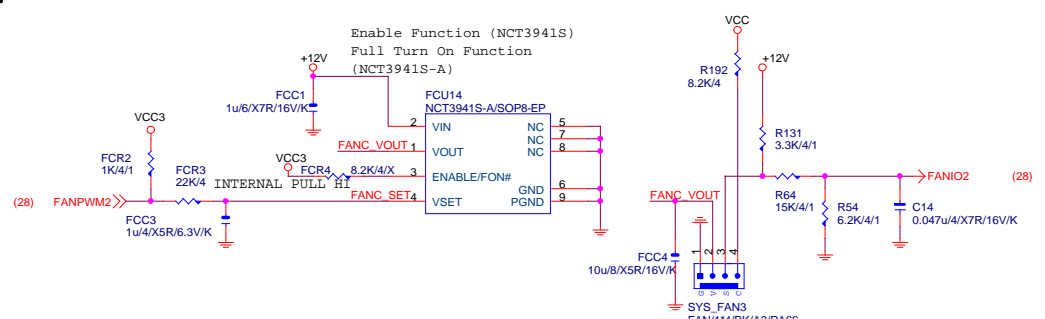
8620 PROCHOT



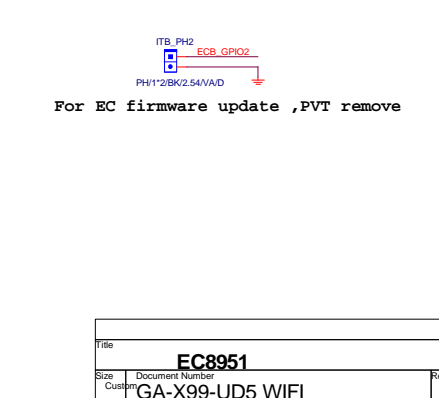
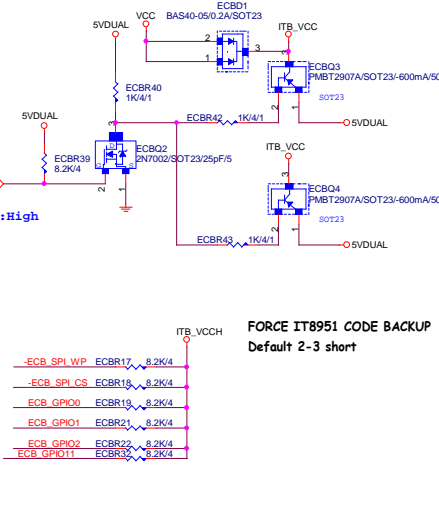
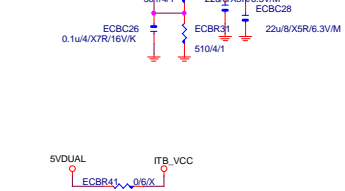
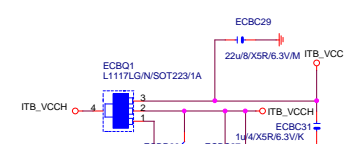
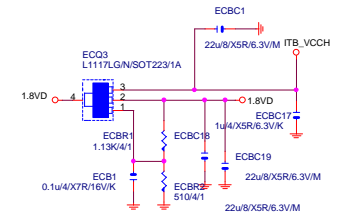
SYS FAN2



SYS FAN3

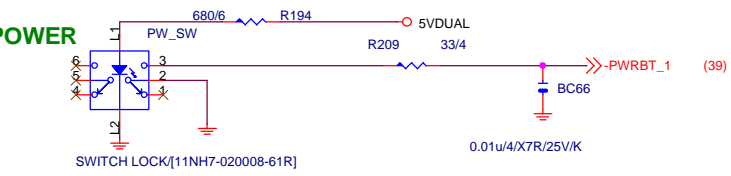


Gigabyte Technology			
Title			
HWM,FAN CTRL			
Size	Document Number	Rev	
Custm		GA-X99-UD5 WIFI 1.1	
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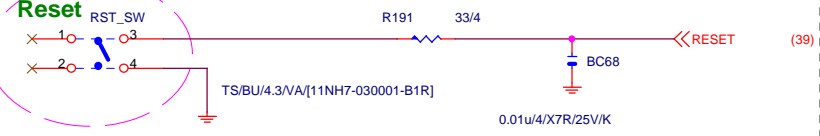


SEL	OE	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

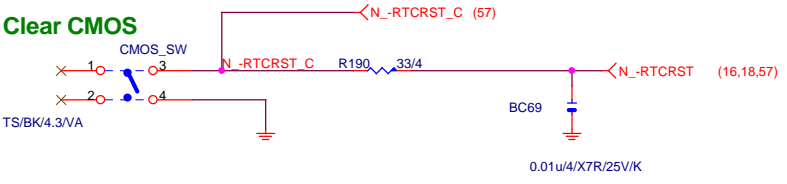
POWER



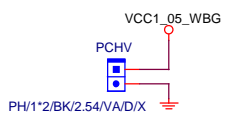
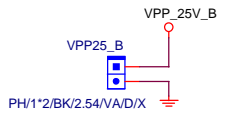
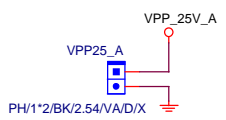
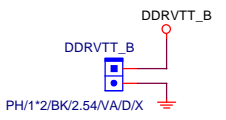
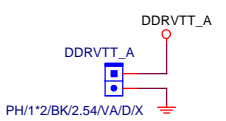
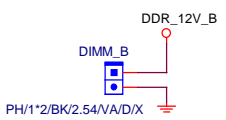
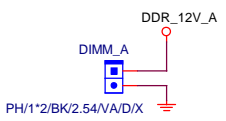
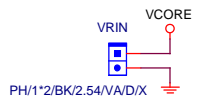
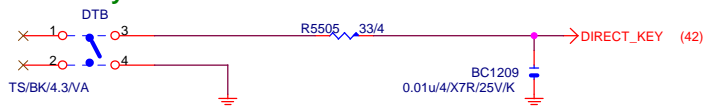
Reset



Clear CMOS

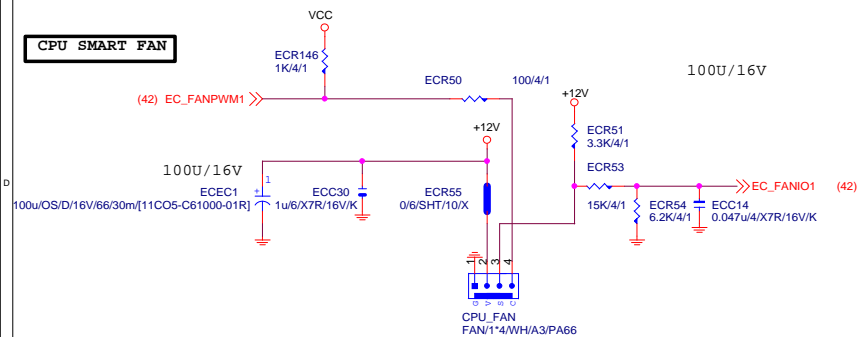


Direct Key

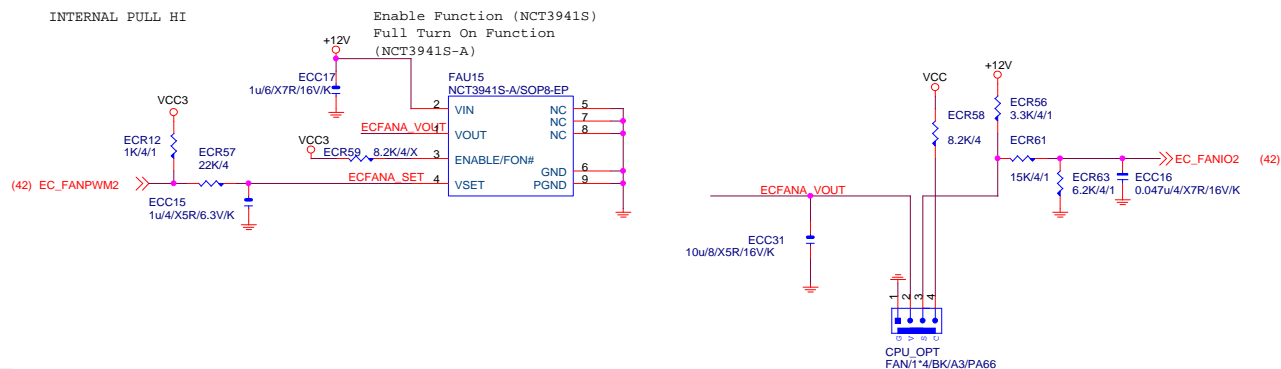


Title			
SWITCH			
Size	Document Number		Rev
B	GA-X99-UD5 WIFI		1.1
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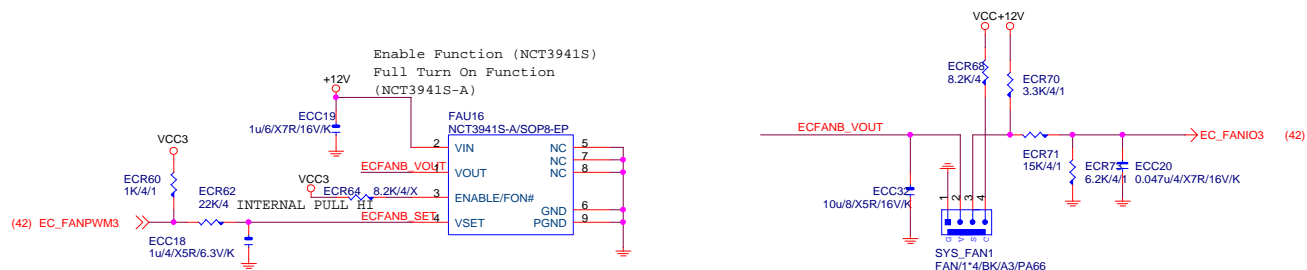
CPU SMART FAN



CPUOPT FAN



SYS FAN1



Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom	GA-X99-UD5 WIFI	1.1	
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SL1000 麥克風輸入電路圖

SLR1 2.2K/4/1/X
2V BIAS

SLR2 4.7K/4/X

SLC1 1u/4/X/5R/6.3V/K/X

SLR3 150K/4/X

SLC2 0.01u/4/X/7R/25V/K/X

SLR4 56K/4/1/X

SLR5 1K/4/1/X

SLR6 330K/4/1/X

SLR7 56K/4/1/X

SLR8 1K/4/1/X

SLR9 1K/4/1/X

SLR10 100K/4/1/X

SLC3 0.1u/4/X/7R/16V/K/X

SLC4 0.1u/4/X/5R/6.3V/K/X

SLC5 22u/8/X/5R/6.3V/M/X

SLC6 22u/8/X/5R/6.3V/M/X

SLU1A LM358DR/SO8/X

SLU1B LM358DR/SO8/X

BAT54A/SOT23/200mA/X

Gain=1+(R1/R2)

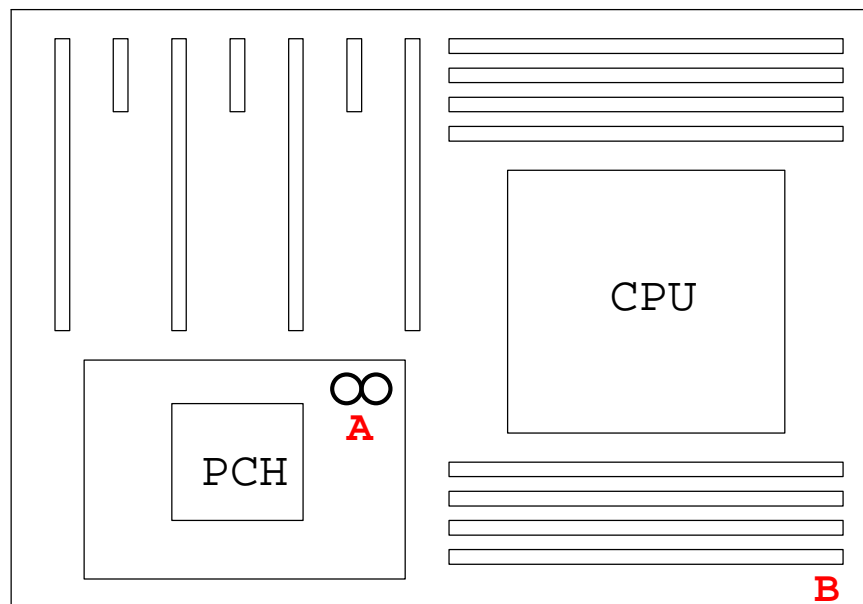
濾成DC

加快放電速度

<=3.3V DC
8620's VIN

[MIC1放在PCH_SINK下, 靠近PCIEX16_1處]

The schematic diagram shows the SLIC2000 microphone preamp circuit. It features a 5V DUAL supply connected to a network of components. A 1M/4X resistor (SLR11) and a 1u4/X5R/6.3V/K/X capacitor (SLC7) are connected in series to ground. The output of this network is connected to the base of a first SOT23 transistor (SLQ1). The emitter of SLQ1 is connected to ground, and its collector is connected to the base of a second SOT23 transistor (SLQ2). The emitter of SLQ2 is connected to ground, and its collector is connected to the output, labeled SL_MIC1_EN. A 8.2K/4/X resistor (SLR12) is connected between the 5V DUAL supply and the output. The output is also connected to a 2N7002/SOT23/25pF/5/X capacitor (SLQ2) to ground.



1. 假設User設定系統噪音要低於45dB(即VINx=1.75V)，當VINx高於1.75V，8620會把PCH的GPI7拉Low一次。
2. 當噪音降低到VINx低於1.65V(即1.75V-0.1V)時，8620會再把PCH的GPI7拉Low一次。
3. 超過Th時，將CPU & VGA降頻或Throttle。低於Tl時，則回復正常頻率運作。

Figure 10.10 illustrates the Interrupt Mode. The graph shows Temperature (Y-axis) versus Time (X-axis). The temperature signal oscillates between levels T_h and T_l . The Interrupt signal is a square wave that transitions from low to high whenever the temperature crosses the T_l threshold from below. Vertical dashed lines mark the points where the temperature crosses the T_l threshold.

1. 麥克風不可被CPU_FAN & VGA_FAN吹到，用DIP電容擋住顯卡的風。
2. 麥克風需和OP-AMP越靠近越好，<1000mil。
3. IT8620偵測到dB值超過user設定值，通知PCH的GPI7發SMI。
4. 麥克風料號為：[10BM1-014030-01R]

dB	VINx
30	1.30V
35	1.45V
40	1.60V
45	1.75V
50	1.90V
55	2.05V
60	2.20V
65	2.35V
70	2.50V
75	2.65V
80	2.80V
85	2.95V
90	3.10V
95	3.25V
100	3.33V

此Table只是假設值，需至無響室測試後確認。

<p align="center">Gigabyte Technology</p>			
<p align="center">Title</p> <p align="center">Sound Level</p>			
<p>Size</p> <p align="center">B</p>	<p>Document Number</p> <p align="center">GA-X99-UD5 WIFI</p>		<p>Rev</p> <p align="center">1.</p>
<p>Date:</p> <p align="center">Monday, December 15, 2014</p>	<p>Sheet</p> <p align="center">46</p>	<p>of</p> <p align="center">64</p>	

請選擇適用的USBport :
SOC/UD7/UD5/G1/G7 : USB3
;UD3/G5:USB5

WIFI use PCIe port4 in X99

DIP螺絲



CR/[12KS2-110202-01R]

SMD螺柱



~CR/[10KS2-040109-01R]
should be SMD level

M_PCIE_H

WIFI_MODULE
WI-FI WITH BT MINI CARD INTEL[20CB1-027260-20R]

PVT need pop this part !

(17) N_+USBP10
(17) N_-USBP10

(17) M2_WIFI_IP
(17) M2_WIFI_IN

(17) CK_WIFI_100M_DP
(17) CK_WIFI_100M_DN

(16,20,21,23,24,25,58) N_-PCI_E_WAKE

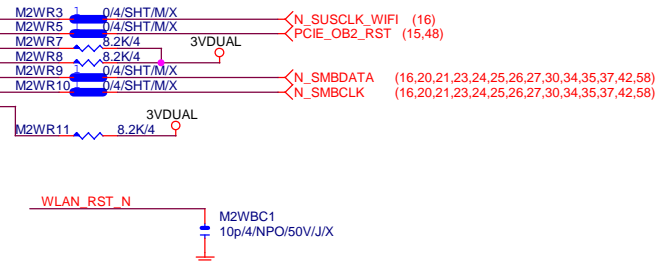
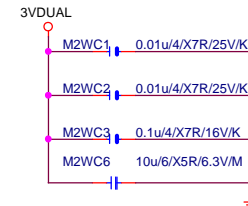
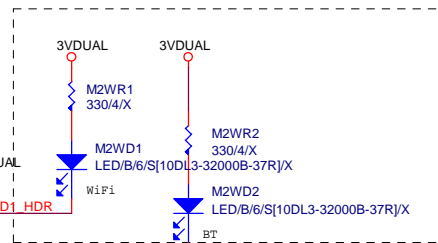
M2_WIFI

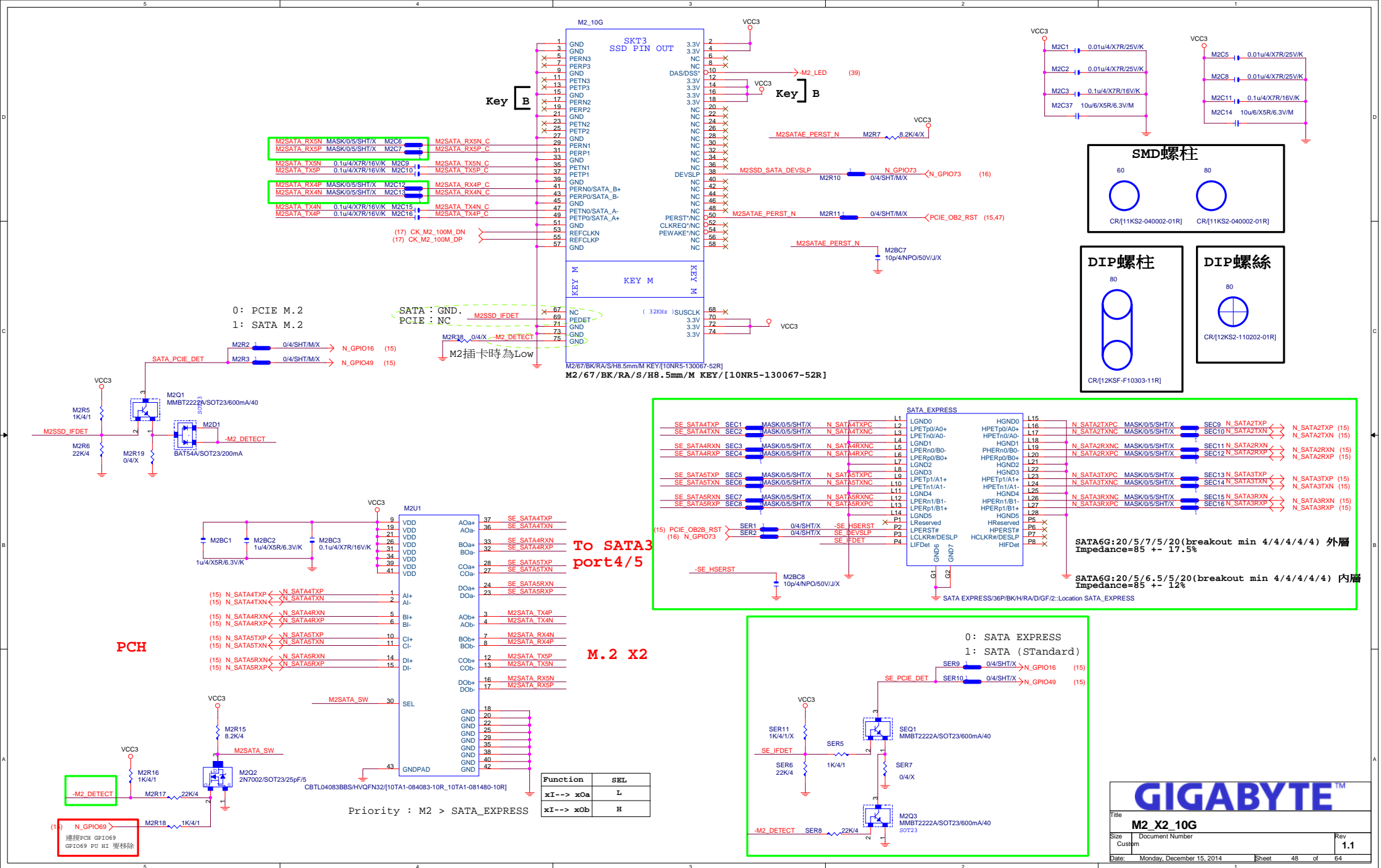
REV=1

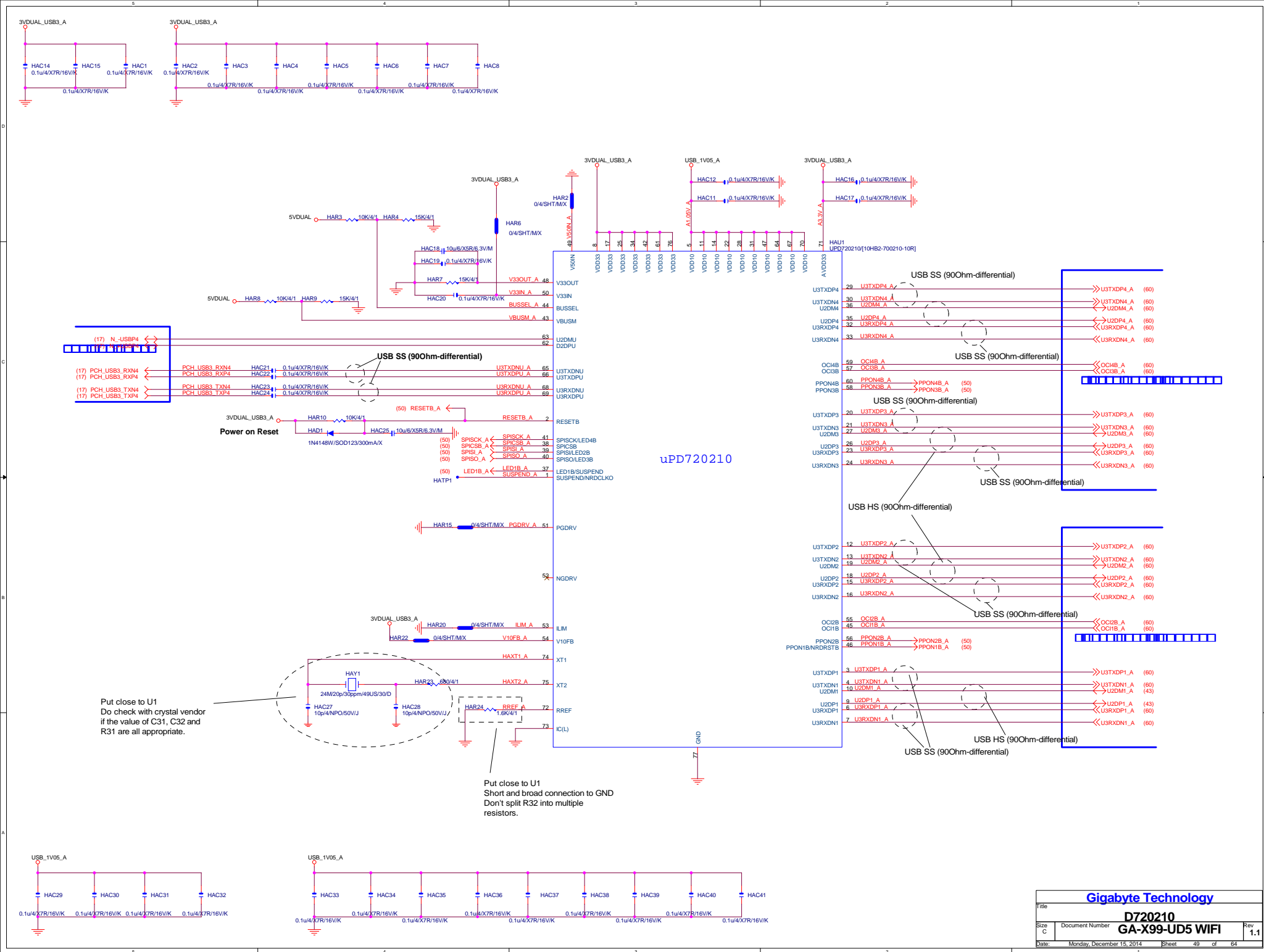
Module Key E

NGFF_M2_E-KEY[10NR5-130067-22R]

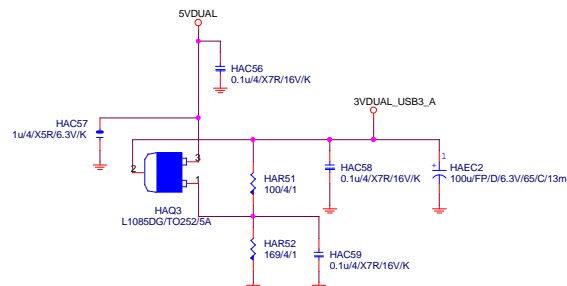
NGFF_M2_E-KEY[10NR5-130067-22R]



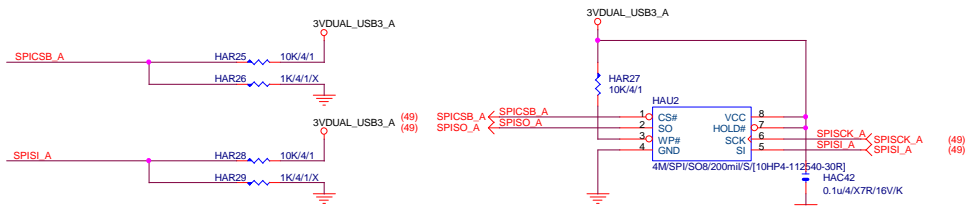




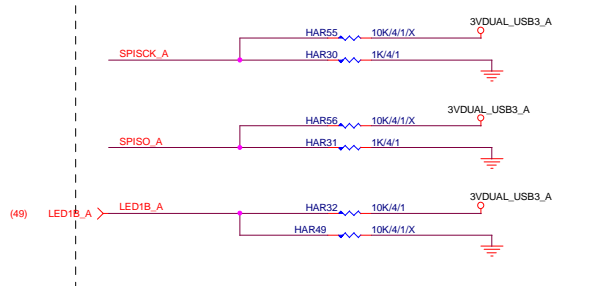
3VDUAL_USB_1



External SPI ROM ; SPI ROM attached mode

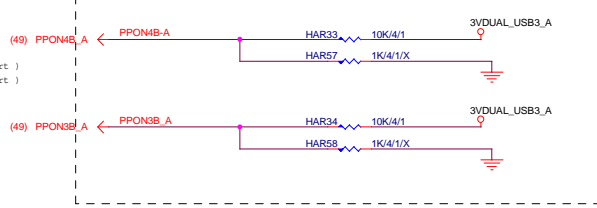


Battery Charging

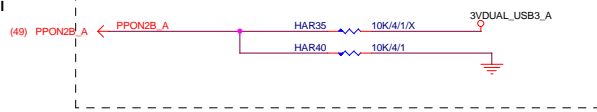


Number of Ports ; 4Ports mode

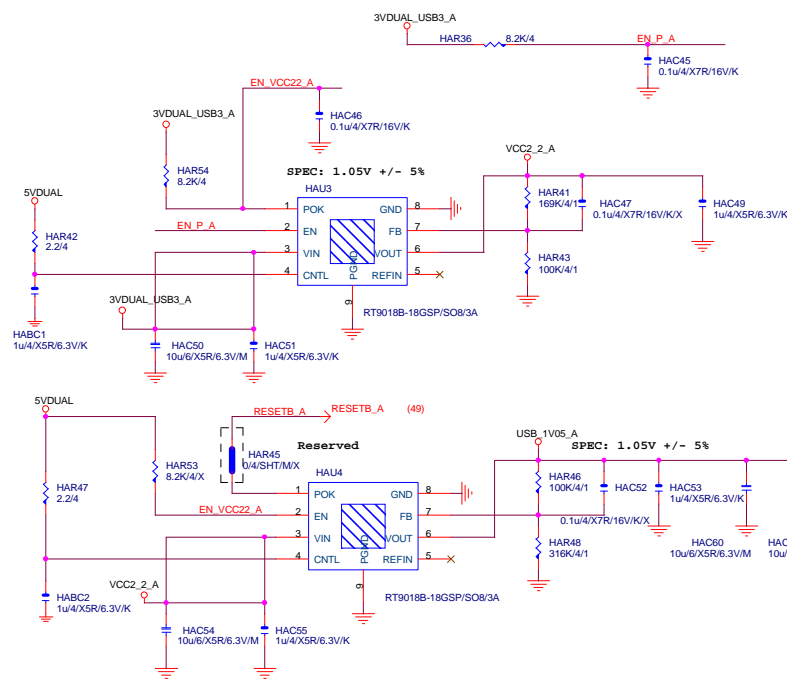
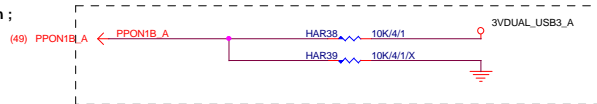
PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)

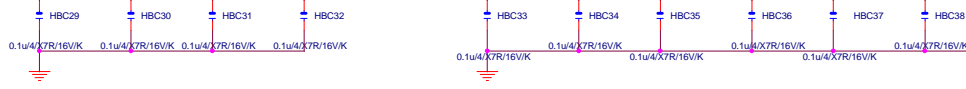
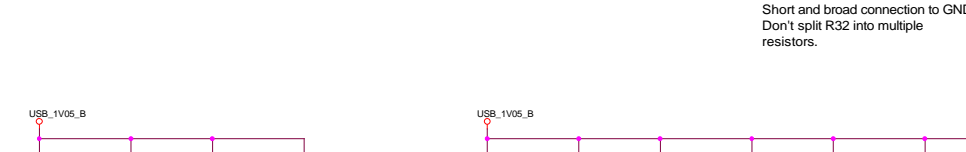
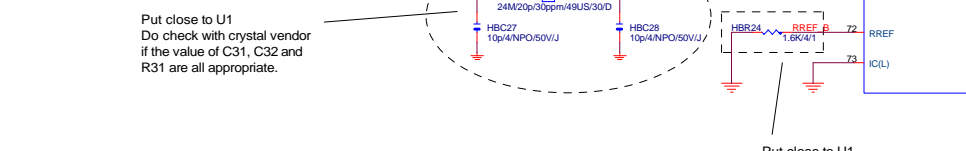
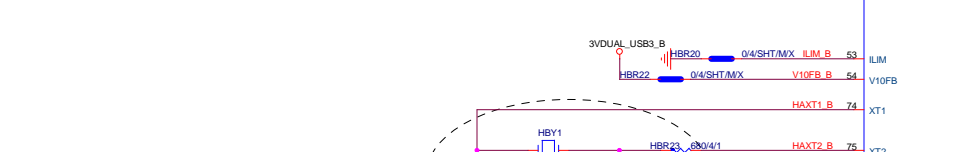
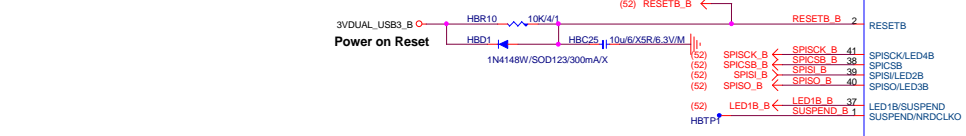
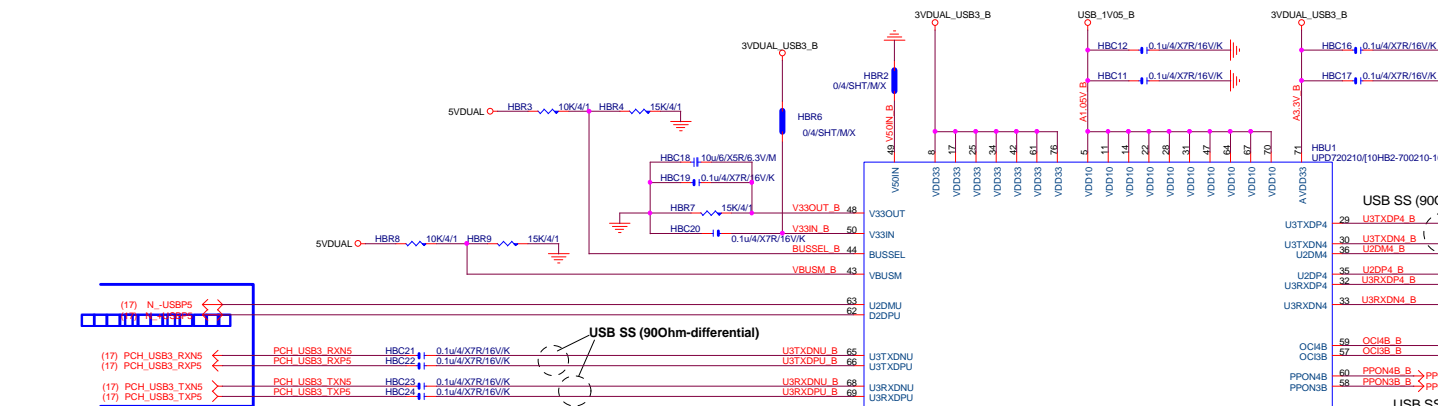
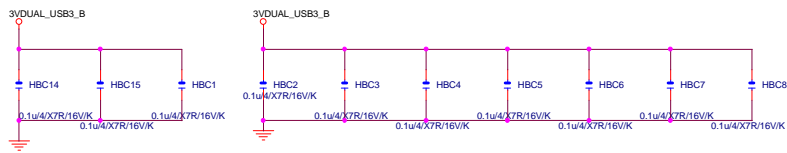


VBUS Power Control ; Individual mode

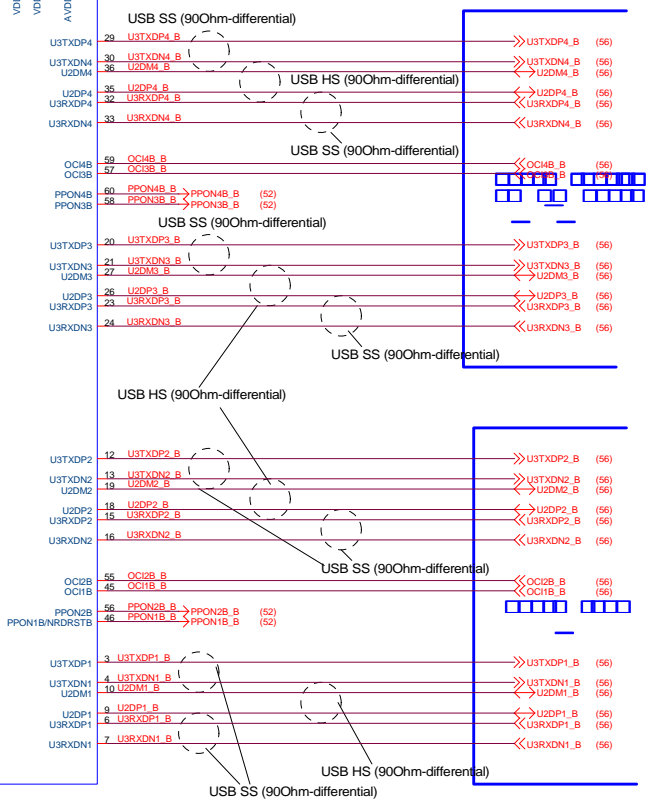


PPON1B Pin Function ; Port1 PPONB mode



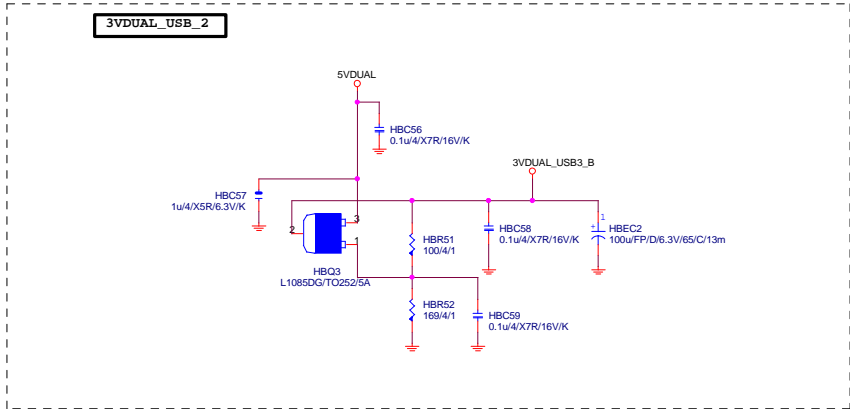


uPD720210

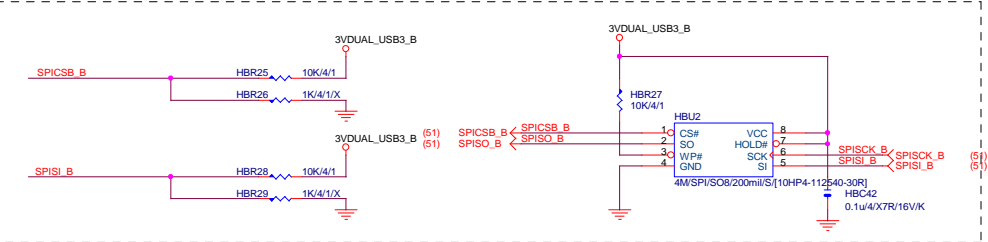


Put close to U1
Do check with crystal vendor
if the value of C31, C32 and
R31 are all appropriate.

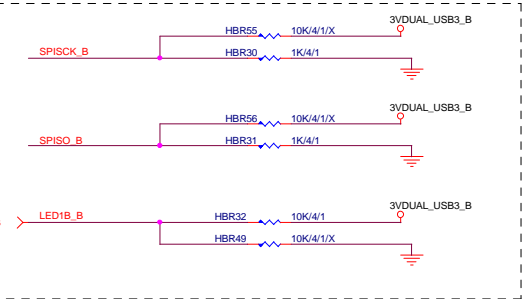
Put close to U1
Short and broad connection to GND
Don't split R32 into multiple
resistors.



External SPI ROM ; SPI ROM attached mode

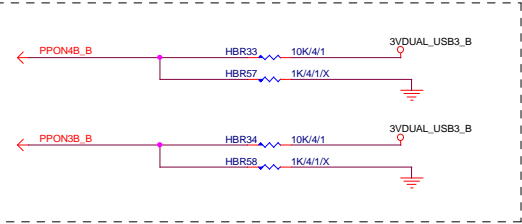


Battery Charging

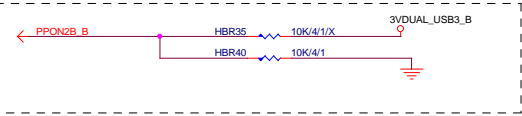


Number of Ports ; 4Ports mode

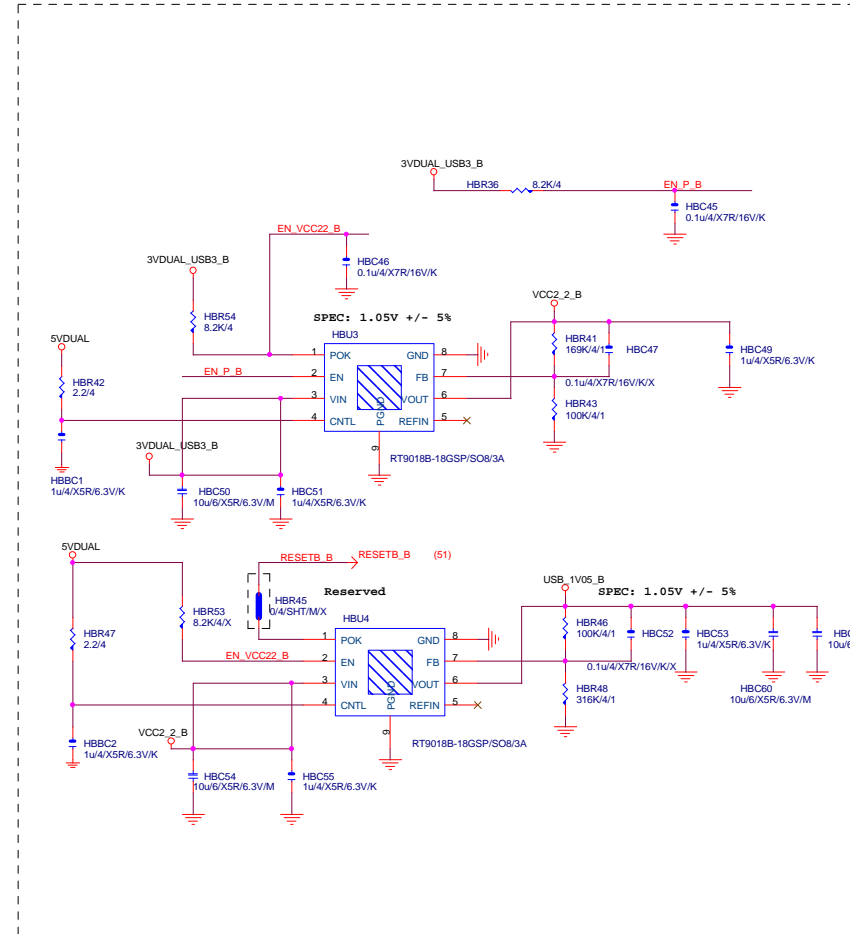
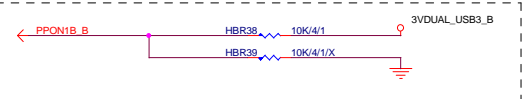
PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)

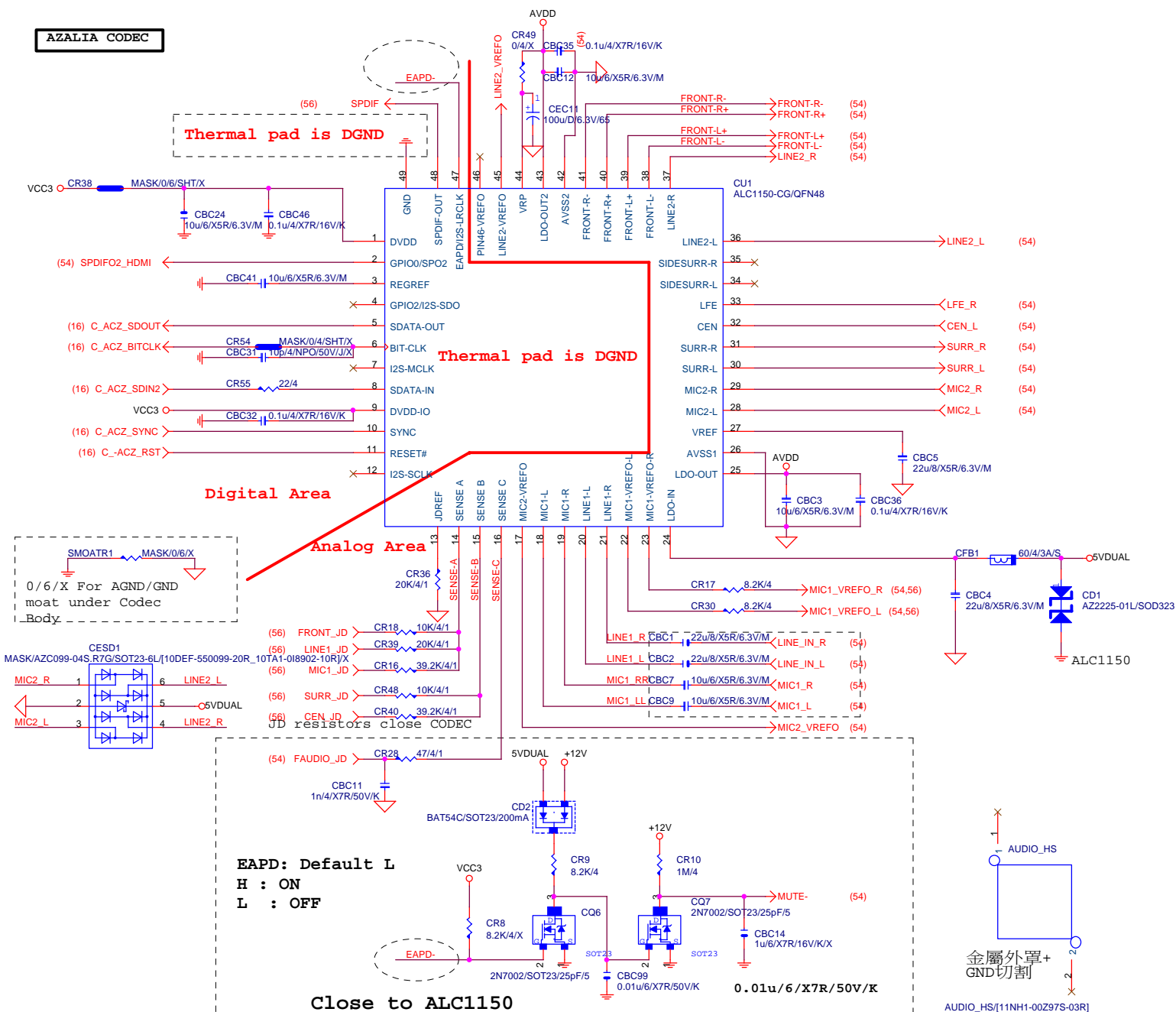


#5 VBUS Power Control ; Individual mode

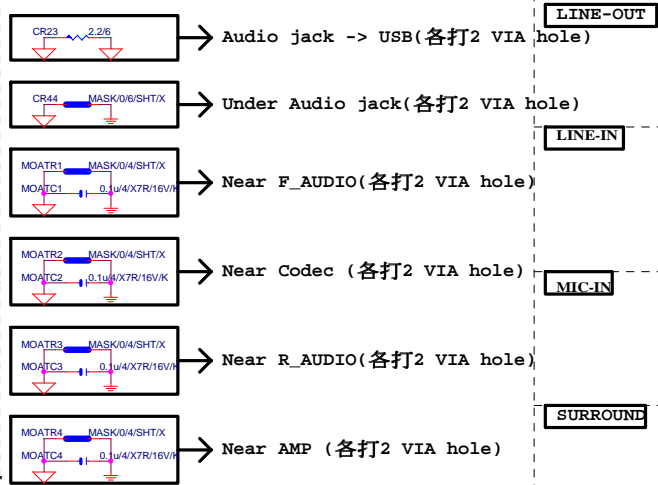


PPON1B Pin Function ; Port1 PPONB mode





金屬外罩+
GND切割



LINE-OUT

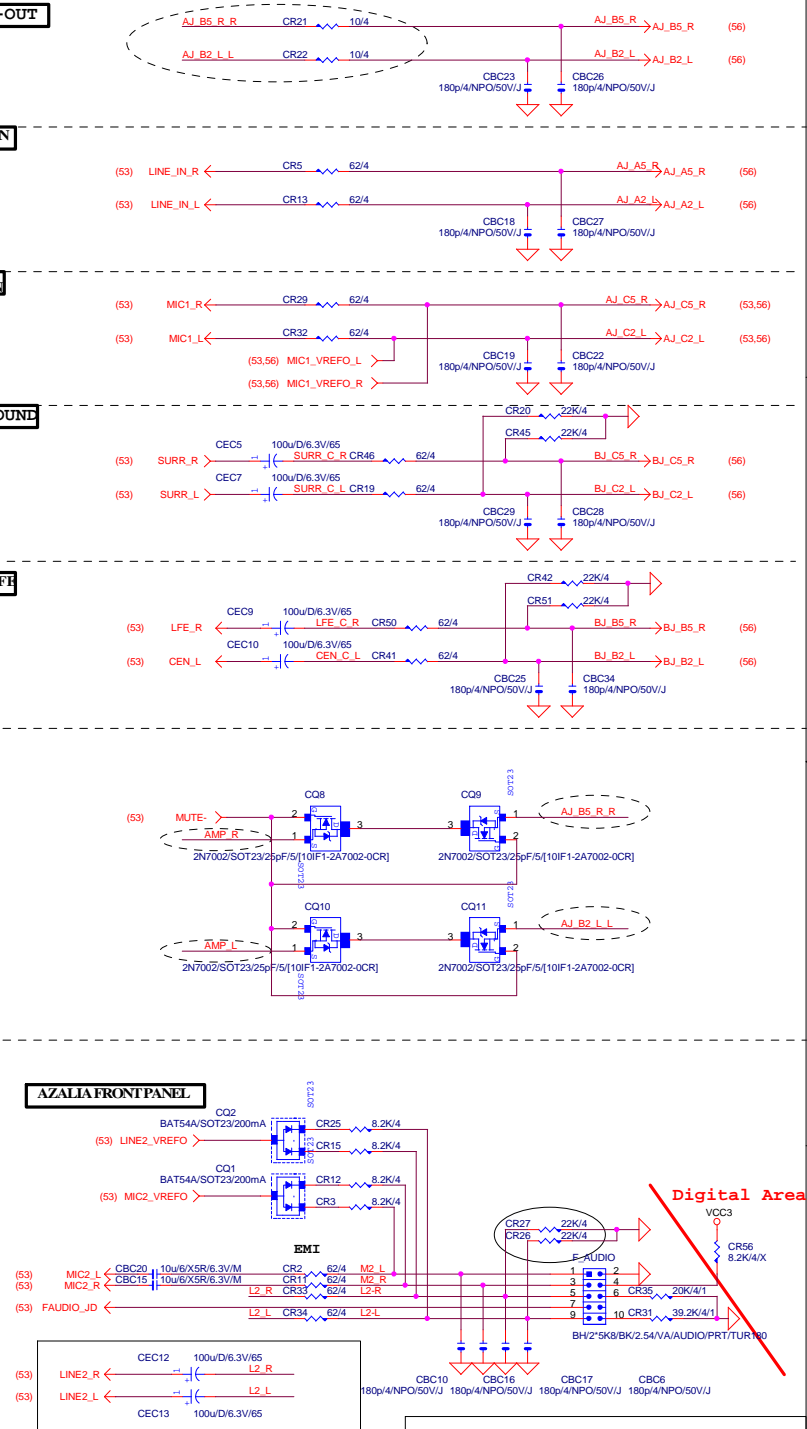
LINE-IN

MIC-IN

SURROUND

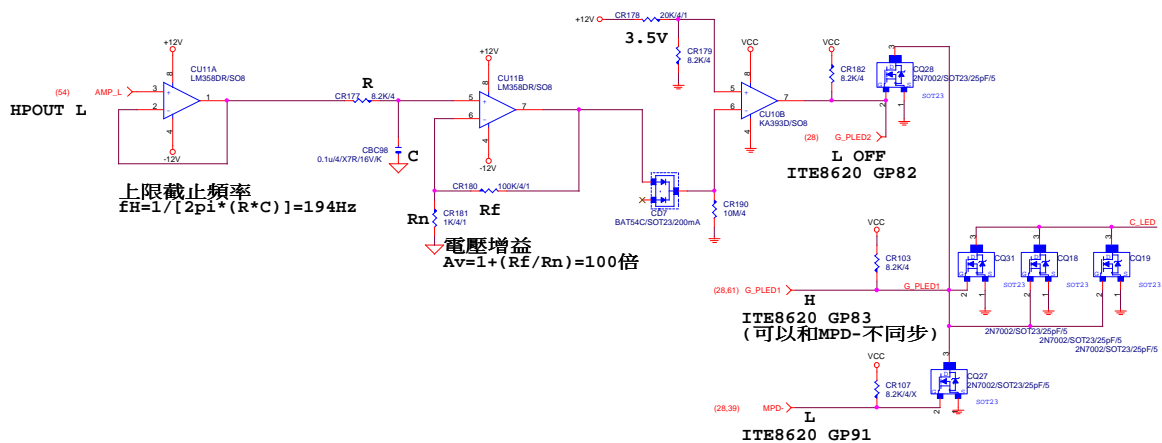
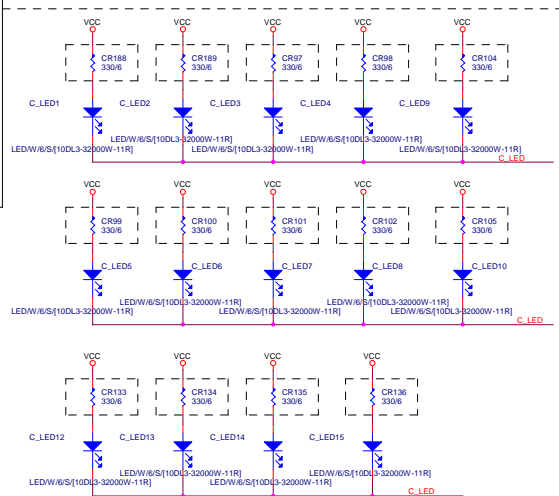
CEN/LFE

AZALIA FRONT PANEL

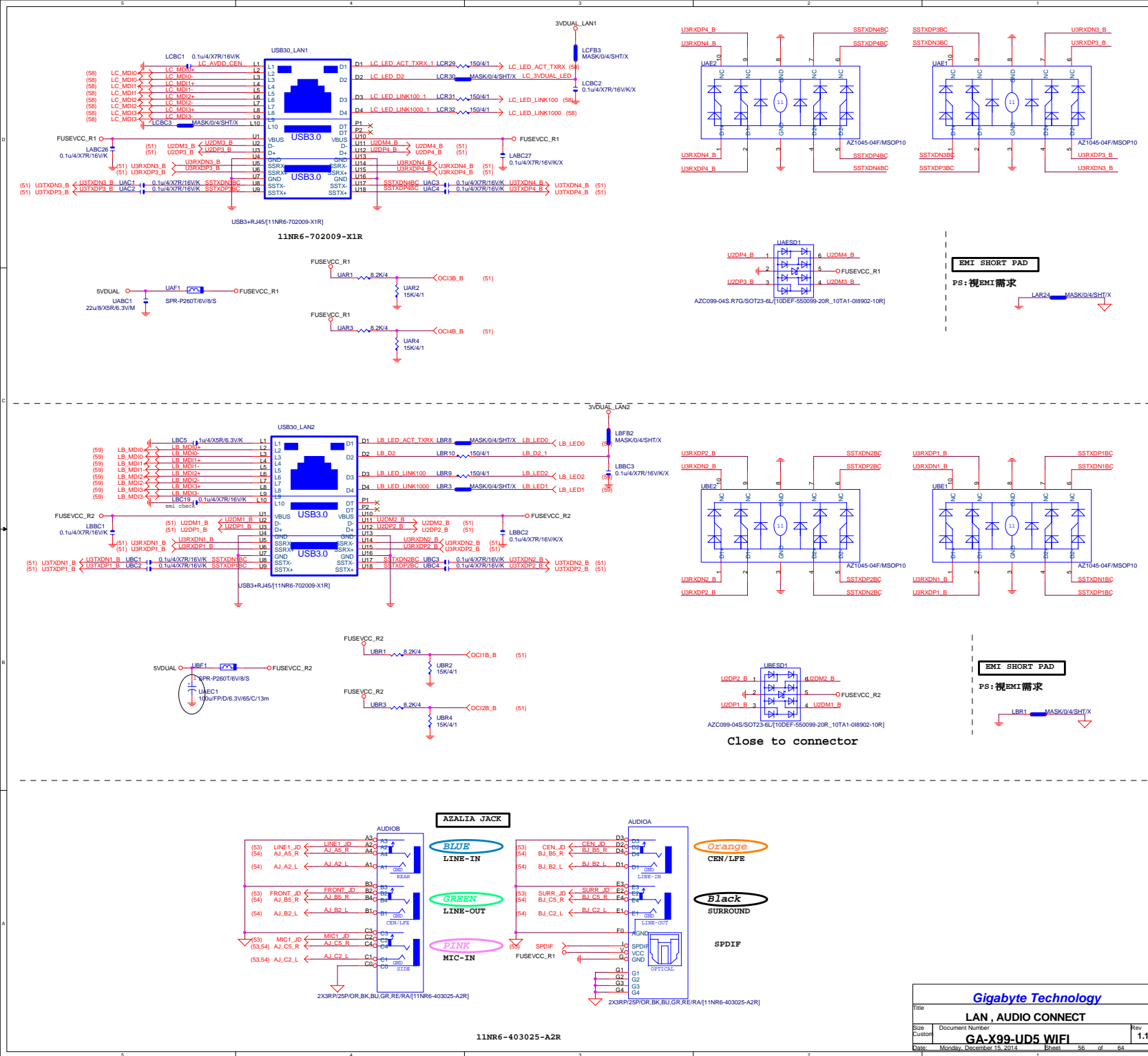


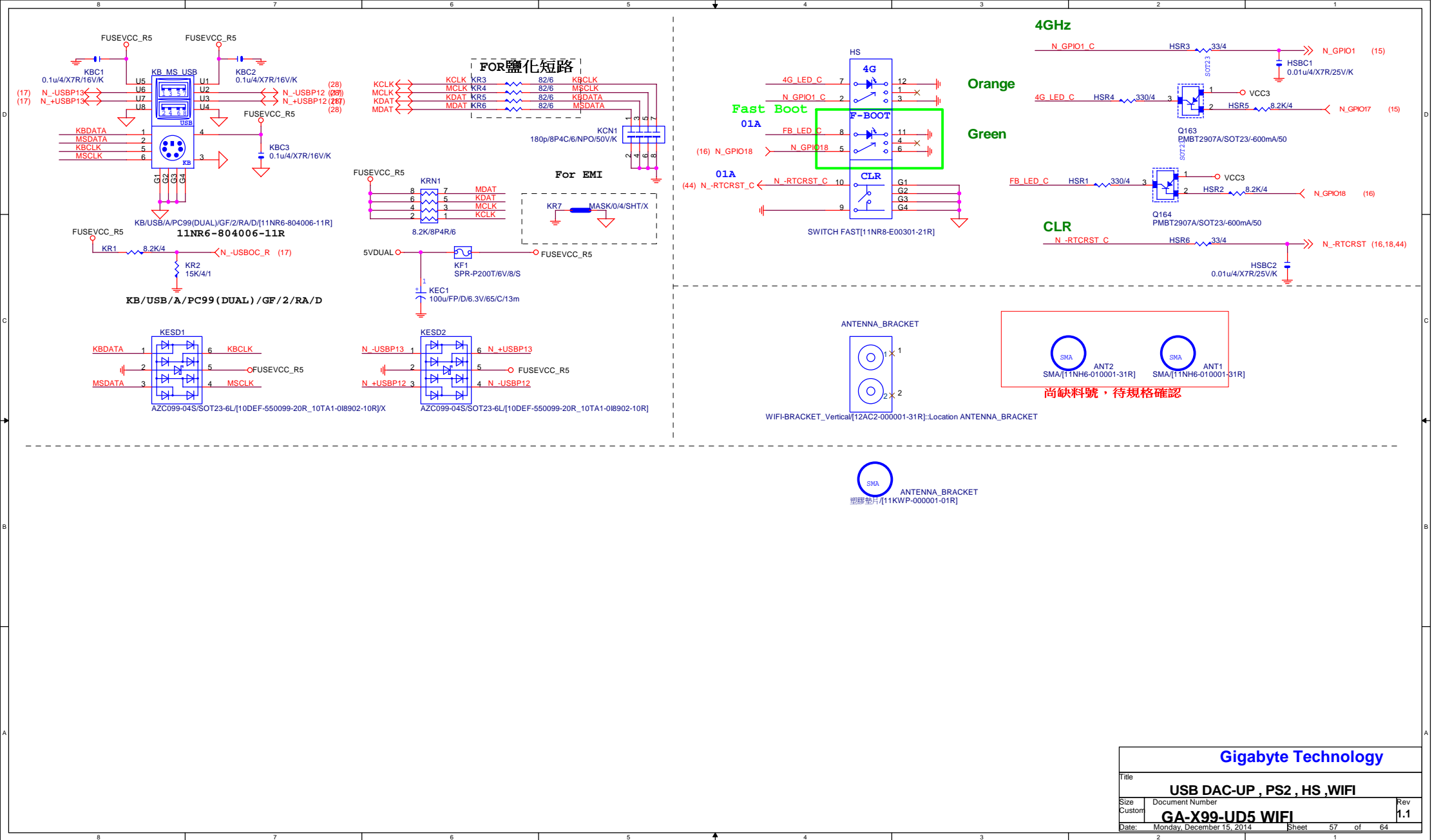
Digital Area

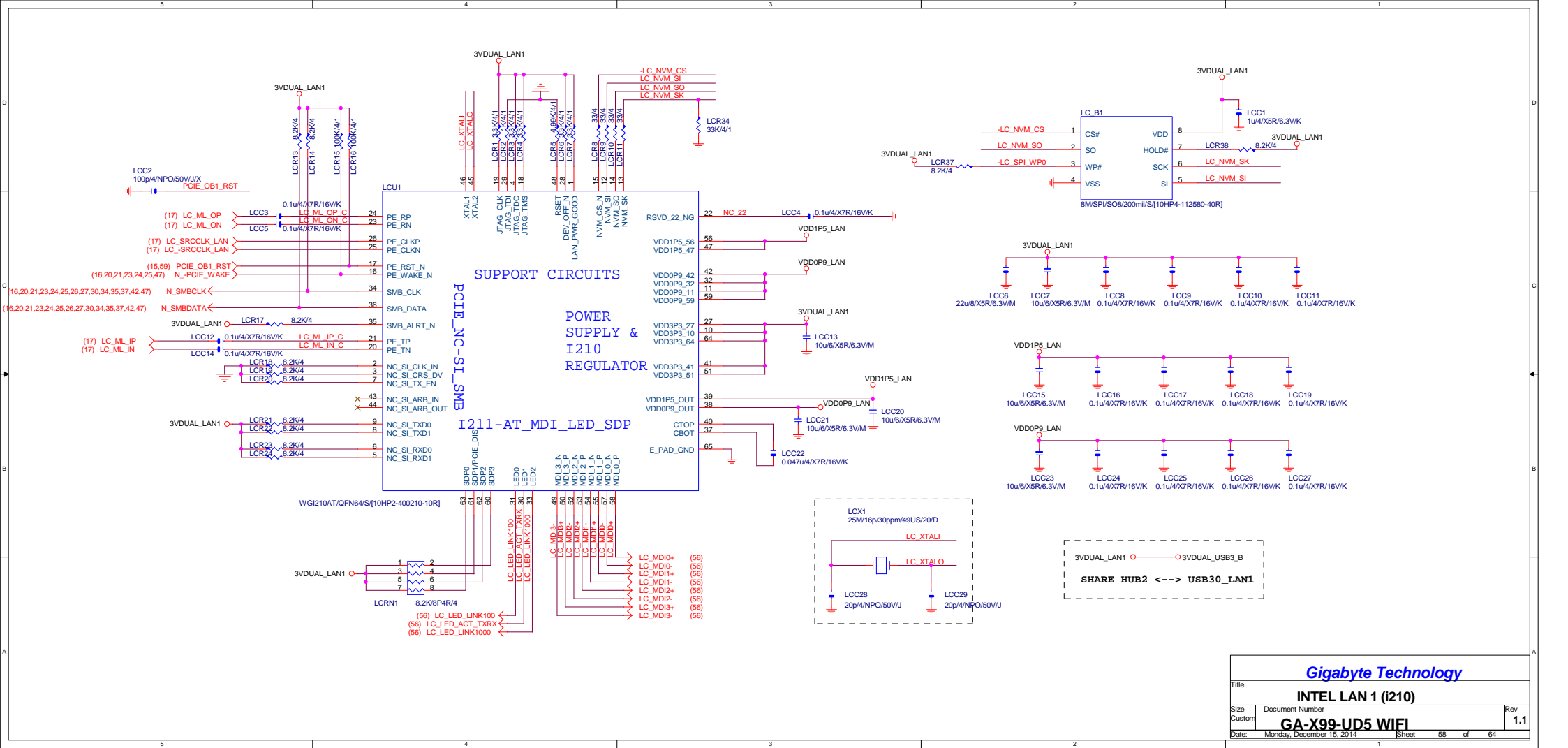
Gigabyte Technology			
Title			
AUDIO JACK			
Size	Document Number		Rev
Custom	GA-X99-UD5 WIFI		1.1
Date:	Monday, December 15, 2014	Sheet	54 of 64

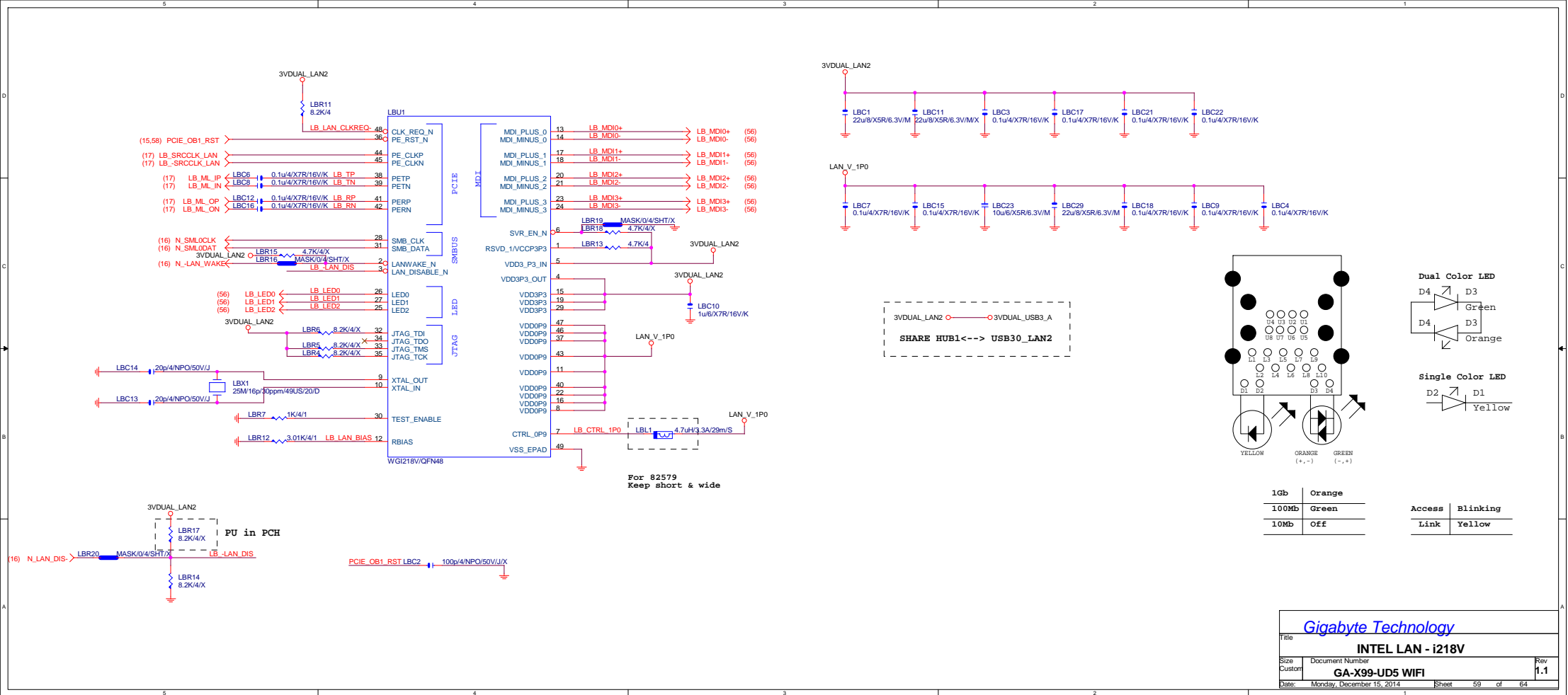


	IO_GP83	IO_GP91	IO_GP82
LED ON	H	L	L
LED OFF	L	L	L
LED BREATH	OD	BREATH	L
LED TEMPO	H	L	OD

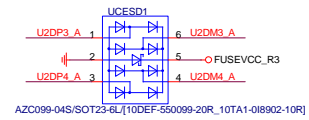
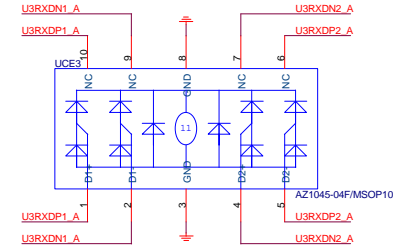
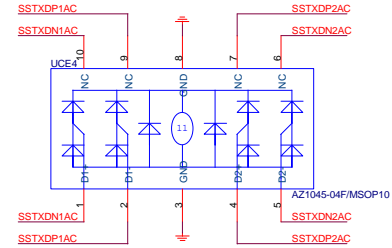
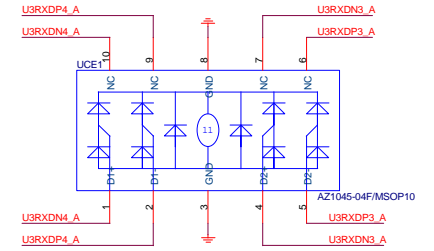
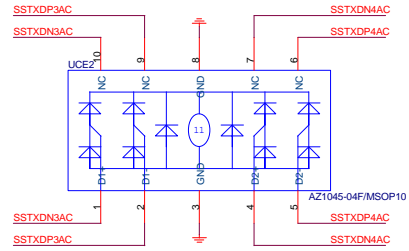
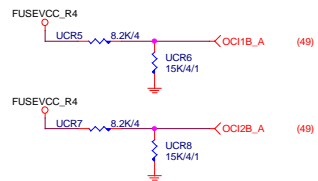
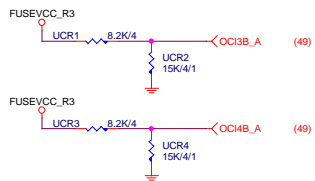
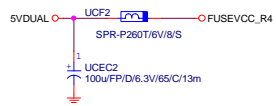
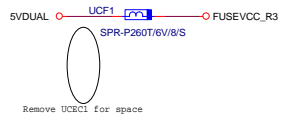
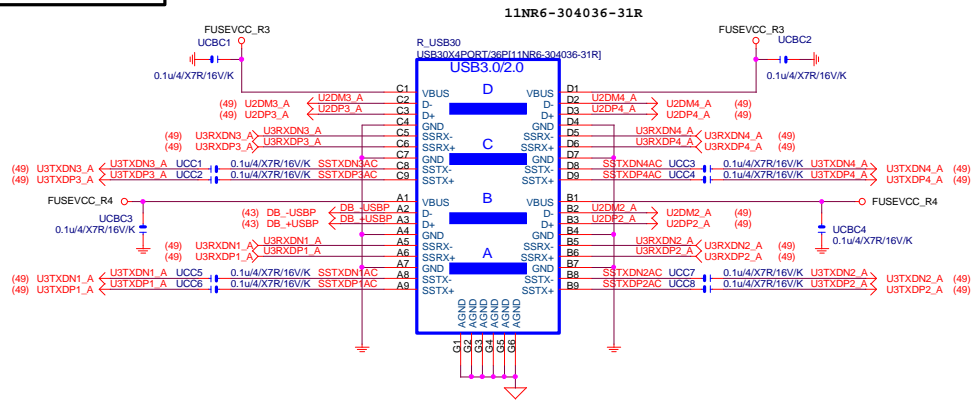




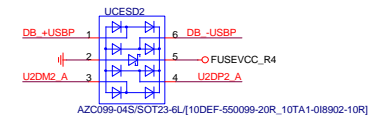




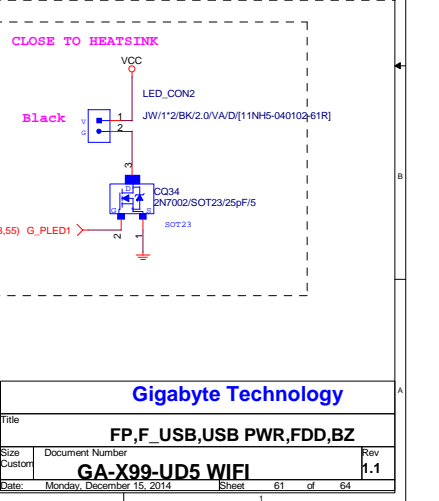
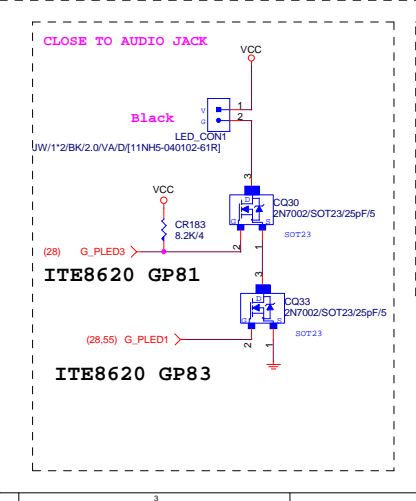
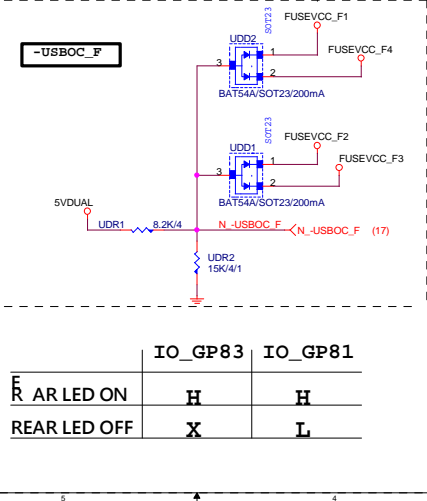
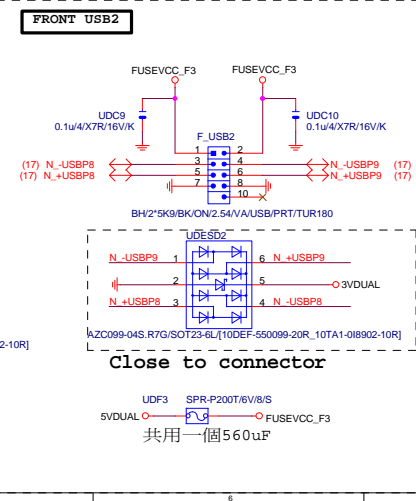
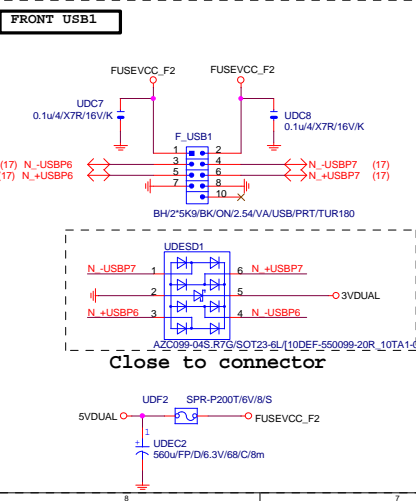
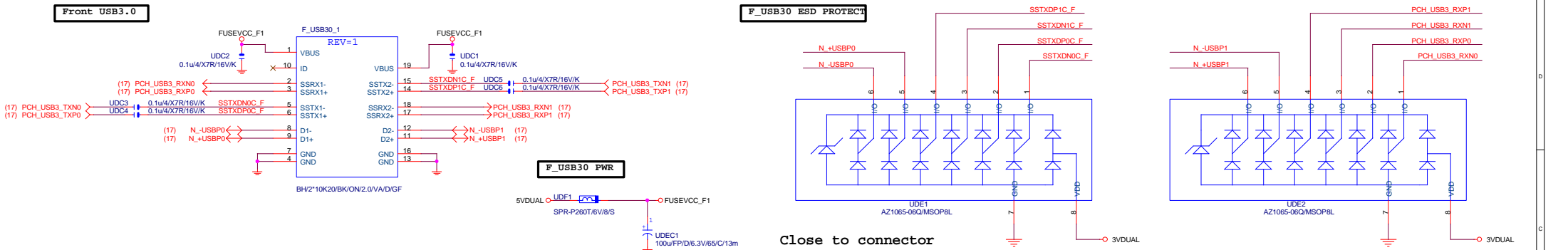
R_USB30 PORT



Close to connector



Close to connector



	IO_GP83	IO_GP81
REAR LED ON	H	H
REAR LED OFF	X	L

PCH GPIO

PIN NAME	POWER WELL	USAGE	AFTER PLTRST	S3/S5	NOTES
GP[0]	VCC3	-ICH_PSI	IN		8.2K P/U TO VCC3
GP[1]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[2]	VCC3	-PIRQE	IN		8.2K P/U TO VCC3
GP[3]	VCC3	-PIRQF	IN		8.2K P/U TO VCC3
GP[4]	VCC3	-PIRQG	IN		8.2K P/U TO VCC3
GP[5]	VCC3	-PIRQH	IN		8.2K P/U TO VCC3
GP[6]	VCC3	GPIO6	IN		8.2K P/U TO VCC3
GP[7]	VCC3	GPIO7	IN		8.2K P/U TO VCC3
GP[8]	3VDUAL	GPIO8	OUT		8.2K P/U TO 3VDUAL
GP[9]	3VDUAL	-USBOC5	IN		USB OVER-CURRENT
GP[10]	3VDUAL	-USBOC6	IN		USB OVER-CURRENT
GP[11]	3VDUAL	GPIO11	IN		8.2K P/U TO 3VDUAL
GP[12]	3VDUAL	GPIO12	OUT		8.2K P/U TO 3VDUAL
GP[13]	3VDUAL	-LPCPME	IN		8.2K P/U TO 3VDUAL
GP[14]	3VDUAL	GPIO14	IN		8.2K P/U TO 3VDUAL
GP[15]	3VDUAL	SPARE	OUT		8.2K P/U TO 3VDUAL (N/A)
GP[16]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[17]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[18]	VCC3	-SPI_WP0	OUT		8.2K P/U TO VCC3
GP[19]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[20]	VCC3	-SPI_WP1	OUT		8.2K P/U TO VCC3
GP[21]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[22]	VCC3	SPARE	IN		1K P/U TO VCC3
GP[23]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[24]	3VDUAL	-SKTOC	IN		8.2K P/U TO 3VDUAL (N/A)
GP[25]	3VDUAL	GPIO25	OUT		8.2K P/U TO 3VDUAL
GP[26]	3VDUAL	SPARE	OUT		8.2K P/U TO 3VDUAL
GP[27]	3VDUAL_PCH	SPARE	OUT		8.2K P/U TO 3VDUAL_PCH
GP[28]	3VDUAL	GPIO28	OUT		8.2K P/U TO 3VDUAL
GP[29]	3VDUAL	SPARE	OUT		8.2K P/U TO 3VDUAL (N/A)
GP[30]	3VDUAL	-S_WARN	OUT		CONNECT TO -S_ACK
GP[31]	3VDUAL_PCH	SPARE	IN		8.2K P/U TO 3VDUAL_PCH(N/A)
GP[32]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[33]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[34]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[35]	VCC3	-ACZ_DET	OUT		8.2K P/U TO VCC3
GP[36]	VCC3	SPARE	IN		8.2K P/U TO VCC3(N/A)
GP[37]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[38]	VCC3	SPARE	IN		1K P/U TO VCC3

PIN NAME	POWER WELL	USAGE	AFTER PLTRST	S3/S5	NOTES
GP[39]	VCC3	SPARE	IN		1K P/U TO VCC3
GP[40]	3VDUAL	-USBOC1	IN		USB OVER-CURRENT
GP[41]	3VDUAL	-USBOC2	IN		USB OVER-CURRENT
GP[42]	3VDUAL	-USBOC3	IN		USB OVER-CURRENT
GP[43]	3VDUAL	-USBOC4	IN		USB OVER-CURRENT
GP[44]	3VDUAL	SPARE	IN		1K P/U TO 3VDUAL
GP[45]	3VDUAL	SPARE	IN		1K P/U TO 3VDUAL
GP[46]	3VDUAL	SPARE	IN		1K P/U TO 3VDUAL
GP[47]	3VDUAL	SPARE	IN		1K P/U TO 3VDUAL
GP[48]	VCC3	SPARE	IN		1K P/U TO VCC3
GP[49]	VCC3	SPARE	IN		8.2K P/U TO VCC3
GP[50]	VCC3	-REQ1	OUT		8.2K P/U TO VCC3
GP[51]	VCC3	-GNT1	OUT		1K P/U TO VCC3
GP[52]	VCC3	-REQ2	OUT		8.2K P/U TO VCC3
GP[53]	VCC3	-GNT2	IN		8.2K P/U TO VCC3(N/A)
GP[54]	VCC3	-REQ3	IN		8.2K P/U TO VCC3
GP[55]	VCC3	-GNT3	IN		8.2K P/U TO VCC3(N/A)
GP[56]	3VDUAL	SPARE	IN		8.2K P/U TO 3VDUAL
GP[57]	3VDUAL	SPARE	IN		8.2K P/U TO 3VDUAL
GP[58]	3VDUAL	SML1CLK	OUT		8.2K P/U TO 3VDUAL
GP[59]	3VDUAL	-USBOC0	IN		USB OVER-CURRENT
GP[60]	3VDUAL	SML0ART	OUT		1K P/U TO 3VDUAL
GP[61]	3VDUAL	SPARE	OUT		8.2K P/U TO 3VDUAL
GP[62]	3VDUAL	SUSCLK	OUT		8.2K P/U TO 3VDUAL(N/A)
GP[63]	3VDUAL	-SLP_S5	OUT		8.2K P/U TO 3VDUAL(N/A)
GP[64]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[65]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[66]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[67]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[68]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[69]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[70]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[71]	VCC3	SPARE	OUT		8.2K P/U TO VCC3
GP[72]	3VDUAL	SPARE	OUT		8.2K P/U TO 3VDUAL
GP[73]	3VDUAL	SPARE	OUT		8.2K P/U TO 3VDUAL
GP[74]	3VDUAL	SML1ART	OUT		1K P/U TO 3VDUAL
GP[75]	3VDUAL	SML1DAT	IN/OUT		8.2K P/U TO 3VDUAL

RS_SYS

LED_CON1

REAR PANEL

PE4_LED

B_BIOS

M_BIOS

PE3_LED

M2_WIFI

M2_20G

M2WD1 M2WD2

PE2_LED

SL_MIC1

PE1_LED

DDR4_4

D4_LED

DDR4_8

D8_LED

DDR4_2

D2_LED

DDR4_6

D6_LED

CPU SOCKET

DDR4_5

D5_LED

DDR4_1

D1_LED

DDR4_7

D7_LED

DDR4_3

D3_LED

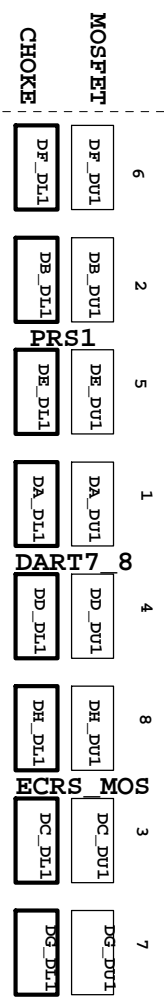
SL_MIC2

PCH
ECRS_PCH
RS_PCH

放在PCH背板正中央

LED_CON2

FBIOS_LED
ECRS_SYS



Gigabyte Technology

Title

Location

Size Document Number

Custom

GA-X99-UD5 WIFI

Rev

1.1

Date: Monday, December 15, 2014 Sheet 63 of 64

